CURRÍCULUM VÍTAE NORMALIZADO

Paul Carpenter

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General quality indicators of scientific research

This section describes briefly the main quality indicators of scientific production (periods of research activity, experience in supervising doctoral theses, total citations, articles in journals of the first quartile, H index...). It also includes other important aspects or peculiarities.

I received my PhD in Computer Architecture from Universitat Politècnica de Catalunya in 2011 (Excel·lent cum Laude). My publication record is:
- Total peer-reviewed publications: 58
- Articles in Q1 journals: 6, with Scopus CiteScore 10.7, 10.2, 8.8, 7.9, 7.9 and 3.8.
- Papers in international CORE A/A* ranked conferences [*]: 16, including MICRO 2012, SC 2013,HPCA 2017, SIGMETRICS 2019, HPCA 2020, SC 2020
- Citations: 1090 (Google Scholar)
- H-index: 16 (Google Scholar)
- i10-index: 23 (Google Scholar)
- Google Scholar: https://scholar.google.es/citations?hl=en&user=V9UomEgAAAAJ

[*] In computer systems, the top international conferences use a rigorous review process with 3 to 7 reviews per paper and acceptance rates of 15% to 25%. The special article, “Best Practices Memo: Evaluating Computer Scientists and Engineers For Promotion and Tenure” (Computing Research News, 1999), states that conference presentations are preferred to journal articles for experimental computer scientists.

My output has increased significantly in recent years. Since the beginning of 2017, I have published 17 peer-reviewed conference publications (8 in CORE A/A* conferences) and 5 Q1 journal articles, and received 335 citations (Google Scholar). As the senior researcher responsible for the research in my group, I am often the last author on my recent publications. I have the following awards directly related to my scientific output:
- IEEE Transactions on Computers 2015 (Scopus CiteScore 2.87) Featured Paper of the Month (1 of 28 papers published)

- Best Paper Award at MEMSYS 2016
- Best Student Paper Award at SC'13 (Microsoft Research h-index 81)
- Best Short Paper Award at PMBS Workshop 2021
- Candidate Best Paper at IEEE LCN 2015 - HiPEAC Paper Award 2012 and 2017

I am principal researcher and first author on 3 international granted patents, all 3 of which have been exploited by ARM products and 1 of which is implemented in ARM Advanced SIMD (>50% of all mobile phones worldwide).

I have received transversal training and acquired skills in project management, time management, writing competitively funded project proposals, negotiation, facilitation, people and team direction, media skills for radio and television, and business plan development.

In addition to myself, my team includes one engineer and 2 PhD students. I have already graduated 6 PhD students and collaborated closely as a co-advisor with 2 additional PhD students.

I am also active in research exploitation, as co-founder of BSC spin-off Talaia Systems, which was finalist in Fundación Repsol Entrepreneurship Fund 2013, as well as research dissemination through 10+ invited talks (including Barcelona Big Data Congress 2016), and 4 videos.

I was engaged in industrial research as external consultant to ARM Research Group, Cambridge, for the period 2003—2005. In this time, I was part of the small multi-disciplinary team (5 people) that designed ARM Advanced SIMD. Advanced SIMD has been successfully exploited, as it is used in close to 50% of all mobile phones worldwide. I was technical lead and primary developer for the ARM MP3 decoder, which was licensed as standard software in several ASSPs (one with >50 design wins) and used by most early portable audio players.

Paul Carpenter

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Nationality:	**United Kingdom**
Country of birth:	**United Kingdom**
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Current professional situation

Employing entity: Barcelona Supercomputing Center

Type of entity: R&D Centre

Department: Barcelona Supercomputing Center

Professional category: Senior Researcher

Educational Management (Yes/No): No

City employing entity: Barcelona, Spain

Start date: 01/09/2014

Dedication regime: Full time

Performed tasks: Leading Microserver Architectures and System Software team, which focusses on runtime system support for distributed memory tasking. Deputy Design and Development Group (DDG) lead and WP3 lead for H2020 DEEP-SEA project (€15 million project). Principal Investigator (PI), Software Technical manager and WP1 lead for H2020 EuroEXA (€20 million project) and FP7 Euroserver Project (137 PMs at BSC). Director / codirector for ten PhD students, and managing one engineer. Member of European Exascale Software Initiative 2 (EESI 2) Working Group on Energy Efficiency. Co-chair of Working Group on Programming Models in EXDCI and the European Technology Platform for High Performance Computing (ETP4HPC) for the 2015 update of the Strategic Research Agenda. ETP4HPC is the main organisation that represents the whole HPC industry and academic within Europe (now 69 members). WP leader for Eurolab-4-HPC WP2 Research. Member of Editorial Team for Rethink Big. Reviewer for IEEE Transactions on Computers (2017), Supercomputing Frontiers and Innovations (2017), Microprocessors and Microsystems (2016) and Scientific Programming (2017). Gave 25 invited talks, member of eight PhD defence/predefence committees.

Applicability in teaching and/or research: Director or codirector for ten PhD students. Eight students have already graduated: Felippe Viera, "Job Scheduling for Disaggregated Memory in High

Performance Computing Systems", graduated October 2023 (Excel·lent; director), Jimmy Aguilar Mena, "Methodology for malleable applications on distributed memory systems", graduated March 2022 (Notable; director), Luis Garrido, "Virtualisation Techniques for the Exploitation of Resources Across Coherence Islands", graduated 2019 (Excel·lent; director), Renan Fischer e Silva, "Interconnect Energy Savings on Microserver Workloads", graduated May 2018 (Excel·lent cum Laude; director), Ugljesa Milic, "Multicore Architecture Optimization for HPC Applications", graduated November 2017 (Excel·lent cum Laude; codirector), Rajiv Nishtala, "Energy Optimizing Methodologies on Heterogeneous Data Centres", graduated July 2017, Karthikeyan Saravanan, "Energy Optimisations in Interconnects for HPC", graduated November 2016 (codirector), and Branimir Dickov, "MPI Layer Techniques to Improve Network Energy Efficiency", graduated December 2015 (Excel·lent cum Laude; codirector). I am currently director of four PhD students: Jimmy Aguilar Mena, started Q1 2017 (director), Luis Garrido, "Virtualisation Techniques for the Exploitation of Resources Across Coherence Islands", started Q2 2014 (director), Omar Ibrahim, "Productive programming of graphs and meshes on distributed memory", started January 2019 (director), and Felippe Vieira, "Managing memory capacity sharing in a supercomputing cluster", started January 2017 (director).

Previous positions and activities

	Employing entity	Professional category	Start date
1	Universitat Politècnica de Catalunya	Senior Researcher	01/11/2011
2	Paul Carpenter Consulting Ltd	Managing Director	08/06/2003
3	ARM	Senior Software Engineer	01/08/1997
4	ARM	Web developer	1996
5	System Interrupt	Developer	1991

1 **Employing entity:** Universitat Politècnica de Catalunya **Type of entity:** University

Professional category: Senior Researcher

Start-End date: 01/11/2011 - 01/09/2014 **Duration:** 2 years - 10 months

Performed tasks: Senior Researcher in the Heterogeneous Architectures Group led by Alex Ramirez (Associate professor). Co-chair of Working Group on Programming Models in the European Technology Platform for High Performance Computing (ETP4HPC), the main organisation that represents the whole HPC industry and academia within Europe (now 64 members: companies, SMEs and research centres). Attended technical workshops during the development of the ETP4HPC Strategic Research Agenda (SRA) in Paris (2012), Munich (2012), Barcelona (2012), Bologna (2012) and Barcelona (2013). Led technical aspects of procurement of the ARM+GPU ("Pedraforca") prototype (budget €700k: 72 nodes with Nvidia Tesla K20 GPUs), including the open call and interactions with the winning supplier (Bull), as well as system performance analysis and project reporting within the FP7 PRACE-1IP project. Full member of HiPEAC Network of Excellence since April 2012. Performed analysis on sustainability of the HiPEAC Network of Excellence, to understand public and private funding of comparable research networking organisations, as well as legal, financial and organisational structure, with presentations and discussions at three physical Steering Committee meetings. Best Paper Award at SAMOS Workshop 2009 and OMHI Workshop 2014; Best Student Paper Award at SC14. HiPEAC Paper Award 2012 (€1,000). Member of IPDPS 2013 Program Committee. Reviewer for Microprocessors and Microsystems (2011), IEEE Transactions on Parallel and Distributed Systems (2012, 2013), ICCD 2012, IEEE IPDPS 2013 PhD Forum, International Journal of Parallel Programming (2011, 2012) and IEEE Access (2014). Reviewed papers for IPDPS 2011, Euro-Par 2012, TACO 2012 and Euro-Par 2013. Attended EU ICT Competitiveness Week 2012 by invitation. Panel member at DATE 2013, "Embedding High Performance Computing: A supercomputer in your pocket or ultra low power exaflop design". One of 200 "promising young researchers" out of ~2,000 applicants selected to spend a week with 24 recipients of the Abel Prize, Fields Medal, Nevanlinna Prize, and ACM A.M. Turing Award at the Heidelberg Laureate Forum 2014. Member of the team led by Alex Ramirez that received the

HiPEAC Technology Transfer Award 2012 for the CARMA (CUDA on ARM) development kit that was productized by SECO. Member of founding team of two serious attempted startups. Finalist in Fundación Repsol Entrepreneurs Fund 2013 for Talaia Systems.
Applicability in teaching and/or research: Delivered Mont-Blanc talks at IS-ENES 2014 (Hamburg), RIKEN AICS 2013 (Tokyo), EU Workshop on strategic directions for next-generation computing 2013 (Brussels), ISCA 2013 (Tel Aviv), LEAP 2013 (London), DATE 2013 (Grenoble), IS-ENES 2013 (Toulouse), and BUX 2012 (Warwick).

2 **Employing entity:** Paul Carpenter Consulting Ltd **Type of entity:** Business
Professional category: Managing Director
Start-End date: 08/06/2003 - 2006
Type of contract: Permanent employment contract
Performed tasks: In 2003, I founded a small consulting company, “Paul Carpenter Consulting Ltd”. The company was incorporated in UK as a limited liability company, with company number 04791370. In addition to the technical responsibilities, I handled VAT [IVA], PAYE payroll and financial reporting. My first consulting opportunity, at ARM, started June 2003, and was extended several times, ending in April 2005. I was part of the small team (<5 people) in the ARM Research Group that designed the ARM Advanced SIMD / NEON vector ISA. It was unusual for ARM to use an external consultant, especially for key IP in the ARM architecture, but few people had the necessary skills. Advanced SIMD is a key part of the ARM architecture, and mandatory in ARMv8-A. It was first introduced in ARM Cortex-A8, in 2005, and the design has changed little as of 2015. This work led to one related worldwide patent. I was author of much of the NEON software training material including the “NEON Code Examples”, RDB01-GENC-003057 (confidential). From July to October 2015, I was engaged at Berkeley Design Technology (BDTI), Inc. in Berkeley, CA. BDTI is respected in the embedded industry as a provider of independent benchmarking and analysis. I performed the analysis for BDTI “Insider Insights on the ARM11’s Signal-Processing Capabilities” (using hardware) and “Assessing Cortex-R4 and Cortex-A8 Signal and Media Processing Performance” (using a cycle-accurate simulator). In addition to providing the technical results and analysis, I delivered a two-day training course about the ARM Architecture and Advanced SIMD to BDTI engineers.

3 **Employing entity:** ARM **Type of entity:** Business
City employing entity: Cambridge, East Anglia, United Kingdom
Professional category: Senior Software Engineer
Start-End date: 01/08/1997 - 01/10/2002 **Duration:** 5 years
Type of contract: Permanent employment contract
Dedication regime: Full time
Performed tasks: Senior Software Engineer. Technical lead for embedded ARM MP3 Decoder (two engineers) and Microsoft Windows Media Audio Decoder (two engineers), both licensed as standard software in several ASSPs (one with >50 design wins), and used by most early portable audio players, including S3 Diamond Rio Receiver, Creative Nomad and Empeg Car. Lead customer on MP3 decoder project recommended us to Microsoft for WMA decoder. Technical lead on Dolby Digital (AC-3) decoder. Handled Dolby certification process, including visit to Dolby Labs in San Francisco, CA; Dolby certification passed first time. Technical lead on MPEG-4 video decoder (three engineers) and development of reusable MOVE video codec components (four engineers). For all projects: feasibility study, development and performance/footprint optimization, programmer's guide (in collaboration with Technical Publications group), ongoing maintenance, training of Support Group (for first level of customer support), advanced customer support via email and phone, technical guidance/training visits for international sales teams, demonstration at annual ARM Partner Meeting (APM) in Cambridge, and accompanying sales on customer visits. Engineering lead for mass storage software segment, involving technical support to business development and analysis of performance and memory footprint. Engineer on V22bis software modem (AS404). Interactions with CPU Architecture team regarding the ARM ISA (usefulness and/or semantics of proposed instructions) and core micro-architecture (choice of multiplier, forwarding paths, etc.). Represented ARM at MPEG-4 Industry Forum (M4IF), Singapore (2001), in order to improve the efficiency of the MPEG-4 video standard on general purpose processors.

Field of management activity: Project manager for MPEG-4 video decoder and for MOVE coprocessor, responsible for successful completion of project within time and budget constraints. Working closely with Product Manager; managing two to four engineers.
Applicability in teaching and/or research: Invented MOVE coprocessor and defined the architecture: an accelerator for video encode (one worldwide patent) which was a standard component on the ARM PrimeXsys Wireless Platform. Internal training on MOVE coprocessor. Performance analysis and memory footprint studies for PVPlayer, Superscape, SolidStreaming, Digital Audio Broadcast (DAB), GSM-AMR, and task parallelism of MPEG-4 Video. Attended six training courses, two technical and four to develop leadership and managerial skills. Worked with ARM's PR company to write an article for EETimes. Co-author of two white papers on the ARM DevZone website. Shadowed the group's representative to the ARM corporate patent review committee. Delivered customer training, including onsite at Sony (Tokyo), Toshiba (Tokyo), Ericsson (Lund, Sweden) and Cirrus Logic (Denver, Colorado).

4 **Employing entity:** ARM **Type of entity:** Business
City employing entity: Cambridge, East Anglia, United Kingdom
Professional category: Web developer
Start-End date: 1996 - 01/08/1997 **Duration:** 2 years
Type of contract: Temporary employment contract
Dedication regime: Part time
Performed tasks: I was the primary developer of the ARM corporate website at www.arm.com. This started as a summer internship, but it continued on a flexible part-time basis during my MA studies. I worked closely with the head of corporate communications, and was included in marketing and branding discussions in the key period leading up to the $1 billion IPO in April 1998. During this time, the website was expanded from a limited site aimed at engineers in companies already in close contact with ARM to target new audiences, including general interest and investors. During this time I made contact with the Software Systems Division and started work on image processing algorithms, which led to permanent employment at ARM.

5 **Employing entity:** System Interrupt **Type of entity:** Business
City employing entity: Bristol, United Kingdom
Professional category: Developer
Start-End date: 1991 - 1993
Dedication regime: Part time
Performed tasks: From approx. 1991 to 1993 I developed Phaethon for Acorn Archimedes. This was initially a personal project, but an early version of the game was discovered by The Serial Port Ltd, and it was launched commercially in December 1993 under the System Interrupt label. Phaethon received positive reviews ("If System Interrupt is going to keep up this standard with future releases, it is soon going to become established as one of the top entertainment labels for Acorn machines", Archimedes World, Jan 1994; "The motion is smooth, fast, and very polished", Acorn Computing, Dec 1993). It is now freely available from Acorn Arcade: http://www.acornarcade.com/forums/viewthread.php?newsid=879. The game was implemented in 17,684 lines of assembler, and it features texture mapped graphics and triple buffering, techniques that were innovative at the time. I published six other small programs as open source in magazines between 1988 and 1992.

Education

University education

1st and 2nd cycle studies and pre-Bologna degrees

1 **University degree:** Higher degree
Name of qualification: Diploma in Computer Science (MA), distinction
City degree awarding entity: Cambridge, United Kingdom
Degree awarding entity: University of Cambridge **Type of entity:** University
Date of qualification: 1997
Average mark: Outstanding
Standardised degree: Yes

2 **University degree:** Middle degree
Name of qualification: BA Hons Mathematics, double first class (Wrangler)
City degree awarding entity: Cambridge, United Kingdom
Degree awarding entity: University of Cambridge **Type of entity:** University
Date of qualification: 1996
Average mark: Outstanding
Prize: Kings Scholarship (twice)
Standardised degree: Yes

Doctorates

Doctorate programme: Arquitectura y tecnología de computadores
Degree awarding entity: Universitat Politècnica de Catalunya **Type of entity:** University
City degree awarding entity: Barcelona, Spain
Date of degree: 24/10/2011
Thesis title: Running Stream-like Programs on Heterogeneous Multi-core Systems
Thesis director: Eduard Ayguade
Thesis co-director: Alex Ramirez
Obtained qualification: Excel·lent cum laude
Standardised degree: Yes

Specialised, lifelong, technical, professional and refresher training (other than formal academic and healthcare studies)

1 **Training title:** Getting Ready for Horizon Europe
Awarding entity: Hyperion Ltd
Training manager: Sean McCarthy
End date: 30/01/2019 **Duration in hours:** 4 hours

2 **Training title:** BSC (Barcelona Supercomputing Center) Innovation Journey
Aims of the entity: The Innovation Journey is a practical program that enables researchers from the BSC to unleash their inner entrepreneur. The program is designed to empower innovators and give them the tools to take their technology out of the science centres and into market. The goal of the Innovation Journey is to unlock new market opportunities, foster connections between the researchers and market leaders, and get more emerging technology into the hands of customers. This six session-long program program offers entrepreneurship training through interactive workshops and experiences as well as mentorship and guidance from established entrepreneurs through a rigorous curriculum.
Training manager: Ricard Garriga
End date: 18/06/2018 **Duration in hours:** 42 hours

3 **Training title:** How to be an Effective Facilitator
Awarding entity: Bernardo Facta Communication **Type of entity:** Business
End date: 28/11/2017 **Duration in hours:** 4 hours

4 **Type of training:** Course
Training title: Coursera Neural Networks for Machine Learning
Awarding entity: Coursera
Training manager: Geoffrey Hinton
End date: 31/07/2017 **Duration in hours:** 24 hours

5 **Training title:** Project Management for non-Project Managers
Awarding entity: Pitagora Group
End date: 26/06/2017 **Duration in hours:** 12 hours

6 **Training title:** Media Skills
Awarding entity: Screenhouse
End date: 28/04/2017 **Duration in hours:** 7 hours

7 **Training title:** Time Management
Awarding entity: Omneom
Aims of the entity: Learn how to increase productivity, reduce stress, and improve results through an effective time management
End date: 30/03/2017 **Duration in hours:** 4 hours

8 **Type of training:** Course
Training title: People and Team Direction
City awarding entity: Barcelona, Catalonia, Spain
Awarding entity: Omneom
Aims of the entity: Familiarise with distinct tools to develop high performing research teams
Training manager: Cesar Llorente
End date: 11/07/2016 **Duration in hours:** 8 hours

9 **Training title:** Heidelberg Laureate Forum (HLF) 2014
City awarding entity: Heidelberg, Germany
Awarding entity: Klaus Tschira Foundation
Aims of the entity: I was an invited participant to the 2nd Heidelberg Laureate Forum (HLF), with worldwide selection and an acceptance rate <10%. The HLF offered all accepted young researchers the opportunity to personally interact with the laureates of the most prestigious prizes in the fields of mathematics and computer science. For one week, the recipients of the Abel Prize, the ACM A.M. Turing Award, the Fields Medal, and the Nevanlinna Prize engaged in a cross-generational scientific dialogue with young researchers.
End date: 26/09/2014 **Duration in hours:** 32 hours

10 **Training title:** How to Write a Competitive Proposal for Horizon 2020
City awarding entity: Barcelona, Spain
Awarding entity: Hyperion Ltd.
Aims of the entity: To train researchers, research managers and research support services in writing professional and competitive proposals for European Commission Horizon 2020.
End date: 16/12/2013 **Duration in hours:** 4 hours

11 **Training title:** Business Plan per a spin offs universitàries
City awarding entity: Barcelona, Spain
Awarding entity: Universitat Politècnica de Catalunya **Type of entity:** University
Aims of the entity: Course aimed at UPC professors to move from technological research to business plan, identify key elements of commercial success and understand the basics of a business plan.
End date: 2012 **Duration in hours:** 8 hours

12 **Training title:** How to Write a Competitive Proposal for Framework 7
City awarding entity: Barcelona, Spain
Awarding entity: Hyperion Ltd.
Aims of the entity: To train researchers, research managers and research support services in writing professional and competitive proposals for European Commission Framework Programme 7.
End date: 11/11/2011 **Duration in hours:** 7 hours

13 **Training title:** 2008 International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES)
City awarding entity: L'Aquila, Italy
Awarding entity: HiPEAC
Aims of the entity: Dissemination of advanced scientific knowledge and the promotion of international contacts among scientists from academia and industry.
End date: 19/07/2008 **Duration in hours:** 48 hours

14 **Training title:** 2007 International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES)
City awarding entity: L'Aquila, Italy
Awarding entity: HiPEAC
Aims of the entity: Dissemination of advanced scientific knowledge and the promotion of international contacts among scientists from academia and industry.
End date: 20/07/2007 **Duration in hours:** 48 hours

15 **Training title:** Riding the waves of mobile phone development
City awarding entity: Bracknell, Berkshire, Buckinghamshire and Oxfordshire, United Kingdom
Awarding entity: ENEA
Aims of the entity: Learn about future of embedded technology within mobile phones and meet industry experts.
End date: 14/06/2005 **Duration in hours:** 5 hours

16 **Training title:** Basics of Building a Business (B3)
City awarding entity: Cambridge, United Kingdom
Awarding entity: Cambridge Entrepreneurship Centre (CEC), Judge Institute of Management Studies, University of Cambridge
Aims of the entity: Basics of entrepreneurship, and how to get started and grow a business. Given by the Judge Institute of Management Studies, ranked 13 worldwide in FT's Global MBA Ranking 2015.
End date: 2003 **Duration in hours:** 12 hours

17 **Training title:** Negotiation Skills
City awarding entity: Cambridge, United Kingdom
Awarding entity: Mentor Group
End date: 10/10/2001 **Duration in hours:** 16 hours

18 **Training title:** 3G Mobile Communication Systems Foundation Course at DSP2000
City awarding entity: London, United Kingdom
Aims of the entity: Fundamentals of 3G communication systems: signal processing for CDMA, FHSS, DSSS, etc.
End date: 07/12/2000 **Duration in hours:** 16 hours

19 **Training title:** MSProject Global v5.0
City awarding entity: Cambridge, United Kingdom
Awarding entity: ARM
Aims of the entity: Project Manager training for MSProject Global v5.0
End date: 27/07/2000 **Duration in hours:** 2 hours

20 **Training title:** Learning the Ropes
City awarding entity: Cambridge, United Kingdom
Awarding entity: Mentor Group
Aims of the entity: Improve communication skills, learn how to match medium with message, practice key influencing strategies, prepare for effective reviews.
End date: 12/07/2000 **Duration in hours:** 24 hours

21 **Training title:** Project Management and ARM Processes
City awarding entity: Cambridge, United Kingdom
Awarding entity: ARM
End date: 17/01/2000 **Duration in hours:** 8 hours

22 **Training title:** Presentation Skills
City awarding entity: Cambridge, United Kingdom
Awarding entity: Mentor Group
End date: 24/11/1999 **Duration in hours:** 16 hours

Language skills

Language	Listening skills	Reading skills	Spoken interaction	Speaking skills	Writing skills
German	A1	A1	A1	A1	A1
Catalan	A2	B1	A1	A1	A1
Spanish	B1	B2	B1	B1	B1
English	C2	C2	C2	C2	C2

Teaching experience

Experience supervising doctoral thesis and/or final year projects

1 **Project title:** Job Scheduling for Disaggregated Memory in High Performance Computing Systems (director; started Jan 2019)
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Felippe Vieira
Date of reading: 09/10/2023
Quality recognition: Yes

2 **Project title:** Methodology for malleable applications on distributed memory systems (director; started Mar 2017)
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Jimmy Aguilar Mena
Date of reading: 23/11/2022
Quality recognition: Yes

3 **Project title:** Virtualisation Techniques for the Exploitation of Resources Across Coherence Islands (director, started 2014)
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Luis Garrido
Obtained qualification: Excel·lent
Date of reading: 26/11/2019
Quality recognition: Yes

4 **Project title:** E-EON Energy-Efficient and Optimized Networks for Hadoop (director; started Jan 2014)
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Renan Fischer e Silva
Obtained qualification: Excel·lent cum Laude
Date of reading: 03/05/2018
Quality recognition: Yes

5 **Project title:** Multicore Architecture Optimizations for HPC Applications
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya
Student: Ugljesa Milic
Obtained qualification: Excel·lente cum Laude
Date of reading: 21/11/2017
Quality recognition: Yes

6 **Project title:** Energy Optimising Methodologies on Heterogeneous Data Centres
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya **Type of entity:** University

Student: Rajiv Nishtala
Date of reading: 10/07/2017
Quality recognition: Yes

7 **Project title:** Energy Optimisations in Interconnects for HPC (co-director)
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Karthikeyan Saravanan
Date of reading: 02/11/2016
Quality recognition: Yes

8 **Project title:** MPI Layer Techniques to Improve Network Energy Efficiency (co-director)
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Branimir Dickov
Obtained qualification: Excel·lent cum Laude
Date of reading: 10/12/2015
Quality recognition: Yes

9 **Project title:** Productive Programming of Irregular Data Structures on Distributed Memory (director; started Jan 2018)
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Omar Ibrahim
Quality recognition: Yes

10 **Project title:** Transparent multi-node dynamic load balancing for MPI+OpenMP applications (director; started Oct 2022)
Entity: Universitat Politècnica de Catalunya
Student: Juliette Fournish d'Albiat

Scientific and technological experience

Research and development groups/teams

1 **Name of the group:** Grupo de Computación de Altas Prestaciones (CAP)
Aims of the group: Investigate technologies that allow improvements in the efficiency of high-performance computing systems. This objective is delivered via diverse perspectives that require a high degree of cooperation: system architecture, compiler, OS, analysis tools, visualization, prediction, algorithms and applications.
Name of principal investigator: Eduard Ayguade
Type of collaboration: Co-authorship of publications
Affiliation entity: Universitat Politècnica de Catalunya **Type of entity:** University
Start date: 01/01/2016

2 **Name of the group:** Microserver architectures and system software
Aims of the group: The microserver architectures and systems software group at Barcelona Supercomputing Center (BSC), which I lead, covers the range between system architecture, system software and runtime systems, with the aim of improving performance and energy efficiency of high-performance computing systems. The major topics of this research group relate to architecture-awareness in the programming model, runtime system and

resource management layers. To date, five PhD students have graduated from the group, and four PhD students and one postdoc are being directed within the group.
Number of members in the group: 6
Affiliation entity: Barcelona Supercomputing Center
Number of directed thesis: 9
Number of directed postdoc: 1
Start date: 01/12/2014
Duration: 4 years

3 **Name of the group:** Heterogeneous Architectures
Aims of the group: To propose new processor designs that provide higher computing performance at lower energy cost, to understand and overcome the challenges in the design of next-generation memory systems for large-scale HPC clusters, and to propose and develop novel methodologies that enable researchers to explore the huge design space represented by future computer architectures.
Name of principal investigator: Jesus Labarta
Number of members in the group: 17
Type of collaboration: Co-authorship of projects and their development
City of group: Barcelona, Spain
Affiliation entity: Barcelona Supercomputing Center
Type of entity: Public Research Body
Number of directed thesis: 12
Number of directed postdoc: 4
Start date: 01/09/2014
Duration: 3 years - 4 months

4 **Name of the group:** ARM Research Group
Aims of the group: Arm Research works in collaboration with academic and industrial partners to explore the latest and most exciting areas of technology affecting [ARM's] industry.
Type of collaboration: Co-authorship of protected modes of technology
City of group: Cambridge, United Kingdom
Affiliation entity: ARM Limited
Type of entity: Business
Start date: 16/06/2003
Duration: 1 year - 10 months

Scientific or technological activities

R&D projects funded through competitive calls of public or private entities

1 **Name of the project:** HiPEAC-7: High Performance, Edge And Cloud computing
Entity where project took place: Barcelona Supercomputing Center
City of entity: Spain
Nº of researchers: 20
Start-End date: 01/12/2022 - 31/05/2025
Participating entity/entities: Barcelona Supercomputing Center ; CEA; Cloudferro; Eclipse Foundation; IDC Italy; INRIA; INSIDE; Rheinisch-Westfaelische Technische Hochschule Aachen; SINTEF; THALES INFORMATION SYSTEMS S.A.; University of Ghent
Total amount: 110.000 €
Applicant's contribution: Leading BSC's contribution to the HiPEAC Vision.

2 **Name of the project:** DEEP-SEA: DEEP – SOFTWARE FOR EXASCALE ARCHITECTURES
Entity where project took place: Barcelona Supercomputing Center
Start-End date: 01/04/2023 - 31/03/2024
Participating entity/entities: BSC; Bayerische Akademie der Wissenschaften; Bull; CEA; ECMWF; ETH Zurich; FORTH; Forschungszentrum Julich; Fraunhofer Gesellschaft; KTH; Katholieke Universiteit Leuven; ParTec; TU Darmstadt; Technische Universitaet Muenchen
Total amount: 1.132.187,5 €

Applicant's contribution: Deputy lead of Design and Development Group (DDG), technical steering body of the project. Lead of WP4: Node-level programming.

3 **Name of the project:** EPEEC: European joint Effort toward a Highly Productive Programming Environment for Heterogeneous Exascale Computing
Type of project: Research and development, including transfer **Geographical area:** European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center **Type of entity:** Public Research Body
Name principal investigator (PI, Co-PI....): Antoniu Peña
Type of participation: Team member
Name of the programme: H2020 FETHPC-02-2017 - Transition to Exascale Computing
Code according to the funding entity: 801051
Start-End date: 01/10/2018 - 30/09/2021 **Duration:** 3 years
Participating entity/entities: Appentra Solutions; Barcelona Supercomputing Center ; CERFACS; CINECA; ETA Scale; Fraunhofer Gesellschaft zur Foerderung der Angewandten Forschung; IMEC; INESC ID; INRIA; Uppsala Universitet
Total amount: 3.990.708,75 €
Dedication regime: Part time
Applicant's contribution: Contributor to Task 4.2: Distributed shared memory support. Responsible for extending the Nanos 6 runtime for remote task execution on the ArgoDSM infrastructure for global shared memory. Information from the Nanos 6 runtime will be used for intelligent prefetching and transparent caching of data.

4 **Name of the project:** LEGaTO: Low Energy Toolset for Heterogeneous Computing
Type of project: Research and development, including transfer **Geographical area:** European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center **Type of entity:** Public Research Body
Name principal investigator (PI, Co-PI....): Osman Unsal
Name of the programme: H2020 ICT-05-2017 - Customised and low energy computing (including Low power processor technologies)
Code according to the funding entity: 780681
Start-End date: 01/12/2017 - 30/11/2020 **Duration:** 3 years
Participating entity/entities: Barcelona Supercomputing Center; Chalmers University of Technology; Christmann Informationstechnik + Medien GmbH & Co KG; Data Intelligence Sweden AB; Helmholtz-Zentrum für Infektionsforschung GmbH; Maxeler Technologies Limited; Technical University of Dresden; Technion; University of Bielefeld; University of Neuchatel
Total amount: 5.514.182,5 €
Applicant's contribution: Contributor to Task 4.2: Programming Model features for energy efficiency: Extension of the OmpSs programming model and Nanos 6 clusters implementation to support irregular data structures needed by the use cases (e.g. graphs). This task is funding the research done by my PhD student Omar Ibrahim.

5 **Name of the project:** EuroEXA
Type of project: Research and development, including transfer **Geographical area:** European Union
Degree of contribution: Scientific coordinator
Entity where project took place: Barcelona Supercomputing Center **Type of entity:** Public Research Body
Name principal investigator (PI, Co-PI....): Paul Carpenter

Funding entity or bodies:
CENTRO DE ACUSTICA APLICADA Y EVALUACION NO DESTRUCTIVA
Type of entity: Associations and Groups

Type of participation: Principal investigator
Code according to the funding entity: 754337
Start-End date: 01/09/2017 - 30/11/2020
Duration: 3 years - 6 months
Total amount: 20.000.000 €
Applicant's contribution: I am the project's Applications and Systems Software Technical Manager, with overall responsibility for the system software (operating system, resource management, parallel filesystem, and run-time systems) and applications (14 production applications from major institutions across Europe, including ECMWF, STFC, BSC, FHG, IMEC, INFN and INAF). I will drive the co-design process in close collaboration with the project's Hardware Technical Manager, as well as the entire project consortium. I am also Workpackage Leader of WP2 Applications, co-design, porting and evaluation, as well as being the project's Principal Investigator at BSC. EuroEXA is one of two proposals funded in the European Commission's FETHPC-01-2016 call, with the ultimate goal of achieving world-class extreme scale capabilities in HPC platforms, technologies and applications. EuroEXA will co-design a balanced HPC architecture for compute- and data-intensive applications using a cost-efficient modular integration approach, demonstrated using key HPC applications from climate/weather, physics/energy and life-science/bioinformatics.

6 **Name of the project:** EXDCI2: European eXtreme Data and Computing Initiative - 2
Type of project: Research and development, including transfer
Geographical area: European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center
Type of entity: Public Research Body
Type of participation: Team member
Name of the programme: H2020 FETHPC-03-2017 - Exascale HPC ecosystem development
Code according to the funding entity: 800957
Start-End date: 01/03/2018 - 21/08/2020
Duration: 2 years - 6 months
Total amount: 2.594.831,25 €
Applicant's contribution: Contributor to Task 4.1: Transversal vision as member of Think Tank contributed to a consensus-based transversal vision on ecosystem-level concepts for HPC in Europe.

7 **Name of the project:** EuroLab4HPC2: Consolidation of European Research Excellence in Exascale HPC Systems
Type of project: Research and development, including transfer
Geographical area: European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center
Type of entity: Public Research Body
Name principal investigator (PI, Co-PI....): Mateo Valero
Name of the programme: H2020 FETHPC-03-2017 - Exascale HPC ecosystem development
Code according to the funding entity: 800962
Start-End date: 01/05/2018 - 30/04/2020
Duration: 3 years
Total amount: 1.600.000 €
Dedication regime: Part time
Applicant's contribution: Acting BSC Principal Investigator on behalf of Mateo Valero (BSC director). Leading Task 1.5 Joint ecosystem activities (to organize two joint activities with the CSA in scope (a) of the same call, EXDCI2), Task 4.3: EUROLAB Vision dissemination (to disseminate the EUROLAB Vision via multiple communication channels), and Task 4.4 EUROLAB Road show (to select events for the EUROLAB Roadshow and run the booth/workshop during the event).

8 **Name of the project:** Computación de Altas Prestaciones VII
Degree of contribution: Researcher
Entity where project took place: Universitat Politècnica de Catalunya
Name principal investigator (PI, Co-PI....): Mateo Valero
Nº of researchers: 54
Name of the programme: MINECO
Code according to the funding entity: TIN2015-65316-P
Start-End date: 01/01/2016 - 31/12/2019
Total amount: 200.355 €

9 **Name of the project:** PREDICT: Prediction of HPC failures in the field
Entity where project took place: Barcelona Supercomputing Center **Type of entity:** Public Research Body
Name principal investigator (PI, Co-PI....): Paul Carpenter; Petar Radojkovic; Mario Nemirovsky
Nº of researchers: 3
Start-End date: 01/04/2019 - 30/06/2019 **Duration:** 3 months
Total amount: 15.000 €
Applicant's contribution: PREDICT is a EuroLab-4-HPC Business Prototyping Project (PPP) to develop a business plan to commercialize BSC's technology in HPC failure prediction and holistic cost/benefit analysis of HPC resiliency. As Entrepreneurial Lead, I will be responsible for leading the BPP through the business prototyping process, meeting with end users, HPC system integrators, OEMs and other stakeholders to understand the value of our technology and to determine the best business model for commercialization.

10 **Name of the project:** ExaNoDe: European Exascale Processor Memory Node Design
Entity where project took place: Barcelona Supercomputing Center **Type of entity:** Public Research Body
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Paul Carpenter
Type of participation: Researcher and Workpackage Lead
Name of the programme: H2020 FETHPC-1-2014 - HPC Core Technologies, Programming Environments and Algorithms for Extreme Parallelism and Extreme Data Applications
Code according to the funding entity: 671578
Start-End date: 01/10/2015 - 30/09/2018
Participating entity/entities: ARM Limited; Bull SAS; Commissariat a l'Energie Atomique et aux Energies Alternatives (CEA); Eidgenössische Technische Hochschule Zürich; Foundation for Research and Technology Hellas; Fraunhofer Gesellschaft zur Förberung der Angewandten Forschung; Scapos AG; The University of Manchester; Virtual Open Systems SARL
Total amount: 8.629.250 €
Applicant's contribution: Leader of WP3 Enablement of Software Compute Node (total 242 PMs). Leader of task to develop programming model and communication library support to address the issues related with building exascale systems from low-power components, including the ExaNode UNIMEM architecture. Leading the work to provide support in OmpSs cluster.

11 **Name of the project:** EuroLab-4-HPC: Foundations of a European Research Center of Excellence in High Performance Computing Systems
Geographical area: European Union
Degree of contribution: Leader Workpackage 2 Research
Entity where project took place: Barcelona Supercomputing Center **Type of entity:** Public Research Body
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Mateo Valero
Name of the programme: H2020 FETHPC-2-2014 - HPC Ecosystem Development
Code according to the funding entity: 671610

Start-End date: 01/09/2015 - 31/08/2017 **Duration:** 2 years
Participating entity/entities: Barcelona Supercomputing Center; Chalmers University of Technology; Eidgenössische Technische Hochschule Zürich; Foundation for Research and Technology Hellas; Ghent University; Institute National de Recherche en Informatique et en Automatique; Rheinisch-Westfälische Technische; Technion; University of Augsburg; University of Edinburgh Edinburgh Parallel Computing Centre; University of Manchester; University of Stuttgart; École Polytechnique Fédérale de Lausanne
Relevant results: EuroLab-4-HPC is a two-year Horizon 2020 project to build the foundation for a European Research Centre of Excellence in High-Performance Computing (HPC) systems. The main objectives are to (a) join HPC system research groups around a long-term HPC research agenda, by forming an HPC research roadmap and joining forces behind it, (b) define an HPC curriculum to foster future European technology leaders, (c) accelerate commercial uptake of new HPC technologies, (d) build an HPC ecosystem of researchers, system providers, VCs etc., and (e) form a business model for the EuroLab-4-HPC excellence centre. Website: www.eurolab4hpc.eu
Applicant's contribution: Leader WP2 Research, which (i) sets a long-term vision for excellence in European academic HPC research, (ii) coordinates efforts to build common research platforms, including multi-disciplinary workshops to address cross-cutting issues and short research stays, and (iii) identifies seeds for innovation and exploitation, as well as mentoring and monitoring of the research projects to accelerate innovations in HPC. Oversaw both calls for cross-site actions, which supported short research visits between European industrial and academic research centres, with the aim of increasing multi-disciplinary collaboration. (Co-)organised workshop at HiPEAC Fall Computing Systems Week 2015 in Milan, "EuroLab-4-HPC: Fostering Excellence in HPC System Research". Overseeing the development of the EuroLab-4-HPC long-term academic roadmap for excellence in European HPC research, covering all layers of HPC computing systems from application to hardware, with a timescale of eight to ten years. Active as the leader of Working Group 2 on System Software and Programming Environment and Working Group 4 on "HPC application evolution and requirements".

12 **Name of the project:** Arquitectura de Computadors d'Altes Prestacions (ACAP)
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center
Name principal investigator (PI, Co-PI....): Mateo Valero
Nº of researchers: 14
Name of the programme: AGAUR. Agència de Gestió d'Ajuts Universitaris i de Recerca
Code according to the funding entity: 2014 SGR 1272
Start-End date: 01/01/2014 - 30/04/2017
Total amount: 65.000 €

13 **Name of the project:** EuroServer - Green Computing Node for European micro-servers
Type of project: Research and development, including transfer **Geographical area:** European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center **Type of entity:** R&D Centre
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Paul Carpenter
Nº of researchers: 29
Type of participation: Principal investigator
Name of the programme: FP7 ICT-2013.3.4 - Advanced computing, embedded and control systems
Code according to the funding entity: 610456
Start-End date: 01/09/2013 - 31/01/2017 **Duration:** 3 years - 5 months
Participating entity/entities: ARM Ltd; Barcelona Supercomputing Center; Chalmers Tekniska Hoegskola; Commissariat a L'Energie Atomique et Aux Energies Alternatives (CEA); Eurotech; Foundation for Research and Technology Hellas (FORTH); OnApp; STMicroelectronics; Technische Universitaet Dresden
Total amount: 12.255.791 €

Relevant results: System architecture and software stack to improve data centre energy-efficiency and cost, by using 64-bit ARM cores, 2.5D heterogeneous silicon-on-silicon integration, FD-SOI, and coherence islands. The architecture will be evaluated using two fully integrated full-system prototypes. Web site: euroserver-project.eu.

Dedication regime: Full time

Applicant's contribution: Principal Investigator (PI) and project leader at BSC (€1.12 M and 137 person-months at BSC). Director of two PhD students: (a) hypervisor support for programming models and (b) interconnect topology and energy proportionality. Leader of dissemination task. Editor and main author of the project's publication at DSD 2014.

14 **Name of the project:** Rethink Big: Roadmap for European Technologies in Hardware and Networking for Big Data

Degree of contribution: Researcher

Entity where project took place: Barcelona Supercomputing Center **Type of entity:** R&D Centre

City of entity: Barcelona, Catalonia, Spain

Name principal investigator (PI, Co-PI....): Adrian Cristal

Name of the programme: ICT-2013.4.2 - Scalable data analytics

Code according to the funding entity: 619788

Start-End date: 01/03/2014 - 28/02/2016

Participating entity/entities: ARM Limited; Alcatel-Lucent Bell Labs France; Barcelona Supercomputing Center; Internet Memory Research SAS; No Rack SAS; Parstream GmbH; Stichting Centrum voor Wiskunde en Informatica (CWI); Technical University of Berlin; Thales SA; The University of Manchester; Universidad Politecnica de Madrid; École Polytechnique Fédérale de Lausanne

Total amount: 2.596.923 €

Relevant results: The objective of the RETHINK big Project is to bring together the key European hardware, networking, and system architects with the key producers and consumers of Big Data to identify the industry coordination points that will maximize European competitiveness in the processing and analysis of Big Data over the next 10 years. Website: rethinkbig-project.eu

Dedication regime: Part time

Applicant's contribution: Member of Editorial team and key role in BSC's coordination of the project.

15 **Name of the project:** HiPEAC-3

Geographical area: European Union

Degree of contribution: Researcher

Entity where project took place: Barcelona Supercomputing Center

City of entity: Barcelona, Catalonia, Spain

Name principal investigator (PI, Co-PI....): Mateo Valero

Nº of researchers: 337

Type of participation: Team member

Name of the programme: FP7-ICT-2011-7

Code according to the funding entity: 287759

Start-End date: 01/02/2012 - 31/01/2016

Participating entity/entities: ARM; Barcelona Supercomputing Center; Chalmers Tekniska Hoegskola; Commissariat a l'Energie Atomique et Aux Energies Alternatives (CEA); Ericsson; Foundation for Research and Technology Hellas (FORTH); IBM Israel - Science and Technology; Institut National de Recherche en Informatique et en Automatique; Recore Systems; Rheinsch-Westfaelische Technische Hochschule Aachen; STMicroelectronics; Thales; Universiteit Gent

Total amount: 3.800.000 €

Relevant results: HiPEAC is a European Network of Excellence (NoE) with the mission to steer and increase European research in the area of high-performance and embedded computing systems. “The HiPEAC network, since its creation in 2004, triggered fundamental changes in the European computing systems community, and it has created a long lasting impact in Europe” (EU Project Officer Panagiotis

Tsarchopoulos). The network stimulates cooperation between a) academia and industry and b) computer architects and tool builders. HiPEAC has 430 members from 275 institutions in 37 countries. Website: hipeac.net

Applicant's contribution: I handled the task to analyse options for self-sustainability of the HiPEAC Network of Excellence, beyond the end of the EU Network of Excellence instrument. This task required an analysis of comparable research organisations, projections of income versus ongoing expenses, and legal, financial and organisational structure. I was also the proofreader for HIPEACinfo quarterly newsletter, which is sent to more than 500 researchers and company managers from academia and industry, in Europe, America and Asia.

16 **Name of the project:** Computación de Altas Prestaciones VI
Entity where project took place: Universitat Politècnica de Catalunya
Name principal investigator (PI, Co-PI....): Mateo Valero
Type of participation: Team member
Start-End date: 01/01/2013 - 31/12/2015

17 **Name of the project:** Mont-Blanc
Geographical area: European Union
Entity where project took place: Barcelona Supercomputing Center
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Filippo Mantovani
Nº of researchers: 30
Type of participation: Team member
Name of the programme: FP7-ICT-2011-7
Code according to the funding entity: 288777
Start-End date: 01/10/2011 - 30/09/2014
Participating entity/entities: ARM Limited; Barcelona Supercomputing Center; Bayerische Akademie der Wissenschaften; Bull SAS; Centre National de la Recherche Scientifique (CNRS); Consorzio Interuniversitario CINECA; Forschungszentrum Jülich GmbH; Gnodal Ltd; Grand Equipement National de Calcul Intensif (GENCI); Universidad de Cantabria
Total amount: 14.500.000 €
Relevant results: Designed new type of computer architecture built from energy-efficient solutions used in embedded and mobile devices. The Mont-Blanc prototype, which is already operational, has 135 nodes, each a dual-core Samsung Exynos 5 with 4 GB RAM, 16 GB uSD, 1 GbE, and Ubuntu 14.04.
Applicant's contribution: Co-advising PhD student researching interconnect energy proportionality. Leading engineer analysing the performance of data centre applications on the Mont-Blanc prototype system. Presented invited talks at IS-ENES 2014 (Hamburg, Germany), RIKEN AICS 2013 (Tokyo, Japan), EU Workshop on strategic directions for next-generation computing 2013 (Brussels, Belgium), ISCA 2013 (Tel Aviv, Israel), LEAP 2013 (London, UK), DATE 2013 (Grenoble, France), IS-ENES 2013 (Toulouse, France), and BUX 2012 (Warwick, UK).

18 **Name of the project:** PRACE-1IP
Type of project: Precompetitive development **Geographical area:** European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center
Name principal investigator (PI, Co-PI....): Sergi Girona
Type of participation: Team member
Name of the programme: FP7-INFRA-20101-2.3.1
Start-End date: 01/07/2010 - 31/12/2013 **Duration:** 2 years
Participating entity/entities: Barcelona Supercomputing Center (BSC); Computation-based Science and Technology Research Center, The Cyprus Institute (CaSToRC); Consorzio Interuniversitario CINECA; Eidgenössische Technische Hochschule Zürich (ETH Zürich); Executive agency “Electronic communication networks and information systems (NCSA); Forschungszentrum Jülich GmbH; GCS – GAUSS Centre

for Supercomputing e.V; Grand Equipement National de Calcul Intensif (GENCI); Greek Research and Technology Network S.A. (GRNET); IT Center for Science Ltd. (CSC); Institute of Physics Belgrade; Johannes Kepler University of Linz (JKU); Laboratory for Advanced Computing of the University of Coimbra (UC-LCA); National University of Ireland, Galway; Poznan Supercomputing and Networking Center (PSNC); SURFsara (formerly SARA Computing and Networking Services); Swedish National Infrastructure for Computing (SNIC); Technical University of Ostrava (VŠB); The Engineering and Physical Sciences Research Council (EPSRC); UNINETT Sigma AS; UYBHM – Ulusal Yuksek Basarimli Hesaplama Merkezi, Istanbul Technical University – National Center for High Performance Computing

Total amount: 27.744.964 €

Relevant results: PRACE (Partnership for Advanced Computing in Europe) was established in 2010 to create a pan-European research infrastructure for world-class supercomputers, and which provides access to the major public supercomputing resources in Europe through an open peer-review process. It also supports users and user communities in porting, scaling and optimising their applications, and provides extensive training through six PRACE Advanced Training Centres (PATC). PRACE-1IP funded the first implementation phase of PRACE, and WP9 explored advanced technologies for next-generation systems by building and evaluating innovative prototype systems.

Applicant's contribution: I led the technical aspects of the procurement of the ARM+GPU prototype, which was part of PRACE's activity to affect the next generation of supercomputers and evaluate technologies that will need multiple iterations to become viable HPC alternatives to the mature contemporary solutions. ARM+GPU ("Pedraforca") has a budget of €700k, and comprised 72 ARM-based nodes, each with an Nvidia Tesla K20 accelerator. This task included defining the open call and interacting with the winning supplier (Bull), as well as performing system performance analysis, and project reporting.

19 **Name of the project:** Computación de Altas Prestaciones V (TIN2007-60625)
Geographical area: National
Degree of contribution: Researcher
Entity where project took place: Universitat Politècnica de Catalunya **Type of entity:** University
City of entity: Barcelona, Spain
Name principal investigator (PI, Co-PI....): Mateo Valero
Nº of researchers: 116
Type of participation: Team member
Name of the programme: Consolider
Start-End date: 10/2007 - 08/2012
Total amount: 3.014.110 €

20 **Name of the project:** ACOTES - Advanced Compiler Technologies for Embedded Streaming
Geographical area: European Union
Degree of contribution: Researcher
Entity where project took place: Departamento de Arquitectura de Computadores (UPC) **Type of entity:** University
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Eduard Ayguade
Nº of researchers: 3
Funding entity or bodies:
Unión Europea **Type of entity:** State agency

Type of participation: Team member
Name of the programme: FP6-2005-IST-5
Code according to the funding entity: 034869
Start-End date: 01/06/2006 - 31/05/2009
Participating entity/entities: Association pour la Recherche et le Développement des Methods et Processus Industriels, Armines; IBM Israel - Science and Technology; Institut National de Recherche en

Informatique et en Automatique (INRIA); NXP Semiconductors Netherlands; STMicroelectronics; Silicon Hive; Universitat Politècnica de Catalunya

Total amount: 5.021.442 €

Relevant results: The ACOTES project worked to increase programmer productivity in the area of streaming applications, through advances in programming model and compiler technology. The programming model introduced C annotations to define the streaming semantics. A source-to-source compiler supported high-level transformations controlled by the partitioning algorithm. The translated program used the Nanos++ runtime system. The project also included work on vectorisation in the GCC backend.

Dedication regime: Full time

Applicant's contribution: Research during PhD studies: abstract model of streaming program and the target hardware (Abstract Streaming Machine). Static partitioning algorithm and static buffer sizing algorithm for the prototype ACOTES compiler. Starsscheck, a tool (based on Valgrind) to check correctness of the annotations. Contributed to project deliverables. Attended ACOTES project meetings in Eindhoven, Netherlands (October 2006) and Haifa, Israel (April 2007), and Cambridge, UK (December 2007).

21 **Name of the project:** EXDCI: European eXtreme Data and Computing Initiative

Geographical area: European Union

Degree of contribution: Researcher

Entity where project took place: Barcelona Supercomputing Center

Name principal investigator (PI, Co-PI....): Sergi Girona

Type of participation: Team member

Name of the programme: H2020 FETHPC-2-2014 - HPC Ecosystem Development

Code according to the funding entity: 671558

Start date: 01/09/2015

Relevant results: EXDCI (European Extreme Data & Computing Initiative) has the objective to coordinate the development of a common strategy for the European HPC ecosystem. The two most significant HPC bodies in Europe, PRACE and ETP4HPC, join their expertise in this 30-month project, which started September 2015. EXDCI is producing and aligning roadmaps for HPC technology and applications, measuring the implementation of the European HPC strategy, and building and maintaining relations with other international HPC activities and regions. Website: exdci.eu.

Applicant's contribution: Co-leader of task related to ecosystem and roadmap towards extreme and pervasive data and computing: high-productivity programming environments and system software. This is an continuation of my role as co-leader of Working Group on Programming Environment for the ETP4HPC SRA, held since 2012.

R&D non-competitive contracts, agreements or projects with public or private entities

1 **Name of the project:** BDTI performance analysis

Type of project: Research and development, including transfer

Entity where project took place: BDTI, Inc.

Degree of contribution: Scientific coordinator

Entity where project took place: BDTI, Inc.

Type of entity: Business

City of entity: Berkeley, United States of America

Name principal investigator (PI, Co-PI....): Paul Carpenter

Nº of researchers: 1

Nª people/year: 1

Participating entity/entities: Paul Carpenter Consulting Ltd.

Start date: 25/07/2005

Duration: 3 months

Relevant results: Performance and memory footprint optimisation and analysis for multimedia codec and BDTI Benchmarks on ARM11 (hardware) and ARM Cortex-A8 processor (cycle-accurate simulator). Delivered two-day training course to BDTI engineers.

2 **Name of the project:** ARM codec representative in development of NEON ISA
Entity where project took place: ARM Holdings PLC
Entity where project took place: ARM Holdings PLC **Type of entity:** Business
City of entity: Cambridge, United Kingdom
Name principal investigator (PI, Co-PI....): Paul Carpenter
Nº of researchers: 1 **Nª people/year:** 1
Participating entity/entities: Paul Carpenter Consulting Ltd.
Start date: 16/06/2003 **Duration:** 1 year - 10 months
Relevant results: Part of the small team (<5 people) in the ARM Research Group (corporate headquarters in Cambridge, UK) that designed the ARM Advanced SIMD / NEON vector ISA. Inventor on one related worldwide patent. Author of NEON software training material (presentation and document "NEON Code Examples", RDB01-GENC-003057). Advanced SIMD was introduced in ARM Cortex-A8 (2005) and the design has changed little as of 2015. Advanced SIMD is mandatory in the latest ARM Architecture (ARMv8-A), and in 64-bit mode it is the only support for SIMD.

3 **Name of the project:** Many consulting projects at ARM (confidential)

Results

Industrial and intellectual property

1 **Title registered industrial property:** Data filtering
Description of qualities: A method, computer program product and data processing apparatus for filtering data, in particular for use in deblocking filters. The method comprising applying a plurality of m filter coefficients which each have a value which is a negative power of two and which sum to one, to a plurality of m input data items to produce a filtered output data item, by performing a sequence of averaging calculations comprising averaging input data items to which a smallest filter coefficient is to be applied to produce first averaged data and averaging the first averaged data with other averaged input data or with input data items to which larger filter coefficients are to be applied the plurality of m filter coefficients being applied to the plurality of m input data items via a sequence of averaging calculations such that a data width of any calculated data does not exceed that of the input data being averaged.
Inventors/authors/obtainers: Paul Matthew Carpenter; Dominic Hugo Symes
Entity holder of rights: ARM Limited
Nº of application: 10/764473
Country of inscription: United States of America
Date of register: 27/01/2004
Conferral date: 01/01/2008
Nº of patent: US7315875 B2
EU patent: Yes
International non-EU patent: Yes
Licences: Yes
Companies: ARM Holdings plc
Products: Implemented in ARM's Video decoder (licenced at least twice), MOVE video components

2 **Title registered industrial property:** Inserting Bits Within a Data Word
Description of qualities: A data processing system (2) is provided which supports shift-and-insert instructions SLI, SRI which serve to shift a source data value by a specified shift amount and then insert bits from that shifted value other than the shifted-in bits into a destination value with the remaining bits within that destination value being unaltered.

Inventors/authors/obtainers: Paul Matthew Carpenter; Simon Andrew Ford
Entity holder of rights: ARM Holdings PLC
Nº of application: PCT/GB2004/003343
Country of inscription: United Kingdom
Date of register: 03/08/2004
Conferral date: 22/06/2006
Nº of patent: WO2005088441 A3
EU patent: Yes
International non-EU patent: Yes **PCT patent:** Yes
Licences: Yes
Products: Exploited in >50% of all mobile phones worldwide, essential part of ARM Advanced SIMD, which is mandatory in ARM's flagship ARMv8-A Architecture and implemented in ARM Cortex-A8,A9,A15,A53,A57, etc.

3 **Title registered industrial property:** Data processing using a coprocessor
Description of qualities: A data processing system using a main processor 8 and a coprocessor 10 provides coprocessor load instructions (USALD) for loading a variable number of data values dependent upon alignment into the coprocessor 10 and also specifying data processing operations to be performed upon operands within those loaded data words to generate result data words. The specified coprocessor processing operations may be a sum of absolute differences calculation for a row of pixel byte values. The result of this may be accumulated within an accumulate register 22. A coprocessor memory 18 is provided within the coprocessor 10 to provide local storage of frequently used operand values for the coprocessor 10.
Inventors/authors/obtainers: Paul Matthew Carpenter; Peter James Aldworth
Entity holder of rights: ARM Limited
Nº of application: WO/2002/067113
Country of inscription: United Kingdom
Date of register: 13/12/2001
Conferral date: 29/08/2002
Nº of patent: WO2002067113 A1
Spanish patent: Yes **EU patent:** Yes
International non-EU patent: Yes **PCT patent:** Yes
Licences: Yes
Companies: ARM Holdings plc
Products: Implemented in ARM's MOVE video accelerator, which was integrated into ARM's PrimeXsys Wireless Platform

4 **Description of qualities:** ARM MP3 Decoder. Technical lead. Licensed as standard software in several ASSPs (one with >50 design wins), and used by most early portable audio players, including S3 Diamond Rio Receiver, Creative Nomad and Empeg Car. Lead customer on MP3 decoder project recommended us to Microsoft for WMA decoder. This product was a major success for the ARM Software Systems Group.
Licences: Yes
Products: ARM AS022

5 **Description of qualities:** ARM Windows Media Audio (WMA) Decoder. Technical lead. Licensed as standard software in several ASSPs (one with >50 design wins), and used by most early portable audio players, including S3 Diamond Rio Receiver, Creative Nomad and Empeg Car.
Licences: Yes

6 **Description of qualities:** Dolby Digital (AC-3) Decoder. Technical lead.
Licences: Yes
Products: AS404

7 **Description of qualities:** MPEG-4 Video Codec. Technical lead. Licenced by ARM and integrated as embedded software in at least two customer ASSPs
Entity holder of rights: ARM
Licences: Yes

8 **Description of qualities:** V22bis Software Modem.
Products: ARM AS404

Scientific and technological activities

Scientific production

Publications, scientific and technical documents

1 Rajiv Nishtala; Vinicius Petrucci; Paul Carpenter; Magnus Sjalander. Twig: Multi-Agent Task Management for Colocated Latency-Critical Cloud Services Latency-Critical Cloud Services. The 26th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2020). 22/02/2020.
Type of production: Scientific paper

2 Rajiv Nishtala; Paul Carpenter; Xavier Martorell. Performance effects on HPC workloads of global memory capacity sharing. MULTIPROG Workshop 2019. 21/01/2019.
Type of production: Scientific paper
Relevant results: 6 pages

3 Renan Fisher e Silva; Paul M. Carpenter. TCP Proactive Congestion Control for East-West Traffic: the Marking Threshold. Computer Networks. Elsevier, 01/01/2019.
Type of production: Scientific paper
Format: Journal
Impact source: SCOPUS
Category: CiteScore
Impact index in year of publication: 3.33
Journal in the top 25%: Yes
Position of publication: 43
No. of journals in the cat.: 259
Relevant results: 11 pages

4 Milan Radulovic; Kazi Asifuzzaman; Darko Zivanovic; Nikola Rajovic; Guillaume Colin de Verdière; Dirk Pleiter; Manolis Marazakis; Nikolaos Kallimanis; Paul Carpenter; Petar Radojkovic; Eduard Ayguadé. Mainstream vs. Emerging HPC: Metrics, Trade-offs and Lessons Learned. Proceedings SBAC-PAD 2018. 24/09/2018.
Type of production: Scientific paper
Relevant results: CORE B conference (acceptance rate: 27%), 12 pages

5 Kyunghun Kim; Antonio J. Peña; Paul Carpenter; Polydoros Petrakis; Manolis Ploumidis; Manolis Marazakis; Yanfei Guo; Kenneth Raffenetti; Pavan Balaji. Toward Developing a Unimem OFI Provider for MPI Support. EuroMPI 2018 poster. 23/09/2018.
Type of production: Scientific paper
Format: Scientific and technical document or report

6 Milan Radulovic; Kazi Asifuzzaman; Paul Carpenter; Petar Radojkovic; Eduard Ayguadé. HPC benchmarking: scaling right and looking beyond the average. Euro-Par 2018. 27/08/2018.
Type of production: Scientific paper
Relevant results: CORE A conference (acceptance rate: 29.4%), 12 pages

7 Adrian Cristal; Osman S. Unsal; Xavier Martorell; Paul Carpenter; Raul De La Cruz; Leonardo Bautista; Daniel Jimenez; Carlos Alvarez; Behzad Salami; Sergi Madonar; Miquel Pericàs; Pedro Trancoso; Micha vor dem Berge; Gunnar Billung-Meyer; Stefan Krupop; Wolfgang Christmann; Frank Klawonn; Amani Mihklafi; Tobias Becker; Georgi Gaydadjiev; Hans Salomonsson; Devdatt Dubhashi; Oron Port; Elad Hadar; Yoav Etsion; Christof Fetzer; Jens Hagemeyer; Thorsten Jungeblut; Nils Kucza; Martin Kaiser; Mario Porrmann; Marcelo Pasin; Valerio Schiavoni; Isabelly Rocha; Christian Göttel; Pascal Felber. LEGaTO: first steps towards energy-efficient toolset for heterogeneous computing. Proceedings of the 18th International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation. 15/07/2018.

Type of production: Scientific paper

Relevant results: 5 pages, 3 citations

8 Karthikeyan Saravanan; Paul Carpenter. PerfBound: Conserving energy with bounded overheads in On/Off-based HPC Interconnects. IEEE Transactions on Computers. IEEE, 07/2018. Available on-line at: <dx.doi.org/10.1109/TC.2018.2790394>. ISSN 0018-9340

Type of production: Scientific paper
Format: Journal
Impact source: SCOPUS
Category: Theoretical Computer Science
Impact index in year of publication: 3.42
Journal in the top 25%: Yes
Position of publication: 9
No. of journals in the cat.: 113

Relevant results: 15 pages, 101 full text views Jan 2018 to Dec 2018 (12 months) in IEEEXplore, 1 citation

9 Luis Garrido; Paul Carpenter. vMCA: Memory Capacity Aggregation and Management in Cloud Environments. Proceedings ICPADS 2017: International Conference on Parallel and Distributed Systems. 15/12/2017. ISSN 1521-9097

Type of production: Scientific paper
Impact source: SCOPUS
Category: Hardware and Architecture
Impact index in year of publication: 0.62
Position of publication: 113
No. of journals in the cat.: 141

Relevant results: 10 pages

10 Rajiv Nishtala; Paul Carpenter; Vinicius Petrucci; Xavier Martorell. The Hipster Approach for Improving Cloud System Efficiency. ACM Transactions on Computer Systems (TOCS). 35 - 3, 12/2017. Available on-line at: <https://doi.org/10.1145/3144168>. ISSN 0734-2071

Type of production: Scientific paper
Format: Journal
Impact source: SCOPUS
Category: General Computer Science
Impact index in year of publication: 4.60
Journal in the top 25%: Yes
Position of publication: 8
No. of journals in the cat.: 200

Relevant results: 25 pages, 403 downloads from ACM Digital Library from Dec 2017 to Jan 2019, 1 citation

11 Luis Garrido; Paul Carpenter. Aggregating and Managing Memory Across Computing Nodes in Cloud Environments. High Performance Computing. ISC High Performance 2017. Lecture Notes in Computer Science. 10524, 20/10/2017. Available on-line at: <https://doi.org/10.1007/978-3-319-67630-2_45>. ISBN 978-3-319-67629-6

Type of production: Scientific paper
Format: Scientific and technical document or report
Impact source: SCOPUS
Category: General Computer Science
Impact index in year of publication: 0.67
Position of publication: 110
No. of journals in the cat.: 191

Relevant results: 10 pages

12 Renan Fischer e Silva; Paul Carpenter. Interconnect Energy Savings and Lower Latency Networks in Hadoop Clusters: The Missing Link. Proceedings of 42nd IEEE Conference on Local Computer Networks (LCN 2017). 09/10/2017. Available on-line at: <http://ieeexplore.ieee.org/document/8109396/>. ISBN 978-1-5090-6523-3

Type of production: Scientific paper

Relevant results: CORE A conference (acceptance rate: 36%), 8 pages, 3 citations

13 Renan Fischer e Silva; Paul Carpenter. Energy Efficient Ethernet on MapReduce Clusters: Packet Coalescing To Improve 10GbE Links. IEEE/ACM Transactions on Networking. 10/2017. Available on-line at: <https://doi.org/10.1109/TNET.2017.2707859>. ISSN 1063-6692

Type of production: Scientific paper
Format: Journal
Impact source: SCOPUS
Category: Software
Impact index in year of publication: 4.23
Journal in the top 25%: Yes
Position of publication: 28
No. of journals in the cat.: 367

Relevant results: 12 pages, 282 full text views June 2017 to Dec 2018 (19 months) in IEEEXplore, 5 citations

14 Renan Fischer e Silva; Paul Carpenter. High Throughput and Low Latency on Hadoop Clusters using Explicit Congestion Notification: The Untold Truth. Proceedings of IEEE Cluster 2017. 05/09/2017. Available on-line at: <https://doi.org/10.1109/CLUSTER.2017.19>. ISSN 2168-9253

Type of production: Scientific paper

Relevant results: CORE A conference (acceptance rate: 31% for short papers), 5 pages, 2 citations

15 Christian Pinto; Kevin Pouget; Daniel Raho; Denis Dutoit; Pierre-Yves Martinez; Chris Doran; Luca Benini; Iakovos Mavroidis; Manolis Marazakis; Valeria Bartsch; Guy Lonsdale; Antoniu Pop; John Goodacre; Annaik Colliot; Paul Carpenter; Petar Radojkovi?; Dirk Pleiter; Dominique Drouin; Benoît Dupont de Dinechin. Paving the way towards a highly energy-efficient and highly integrated compute node for the Exascale revolution: the ExaNoDe approach. 2017 Euromicro Conference on Digital System Design (DSD). 30/08/2017. Available on-line at: <https://doi.org/10.1109/DSD.2017.37>. ISBN 978-1-5386-2145-5

Type of production: Scientific paper

Relevant results: 8 pages, 5 citations

16 Ugljesa Milic; Alejandro Rico; Paul Carpenter; Alex Ramirez. Sharing the Instruction Cache Among Lean Cores on an Asymmetric CMP for HPC Applications. Proceedings 2017 IEEE International Symposium on Performance Analysis of Systems & Software (ISPASS). IEEE, 24/04/2017. Available on-line at: <https://doi.org/10.1109/ISPASS.2017.7975265>. ISBN 978-1-5386-3889-7

Type of production: Scientific paper
Format: Scientific and technical document or report
Corresponding author: No

Relevant results: CORE C conference, 10 pages, 2 citations

17 Darko Zivanovic; Milan Radulovic; Hyunsung Shin; Jongpil Son; Sally A. McKee; Paul M. Carpenter; Petar Radojkovic; Eduard Ayguade. Main Memory in HPC: Do We Need More, or Could We Live With Less?. ACM Transactions on Architecture and Code Optimization (TACO). 14 - 1, 04/2017. Available on-line at: <https://doi.org/10.1145/3023362>. ISSN 1544-3566

Type of production: Scientific paper
Format: Journal
Impact source: SCOPUS
Category: Hardware and Architecture
Impact index in year of publication: 1.42
Position of publication: 54
No. of journals in the cat.: 139

Relevant results: 25 pages, 6 citations, 684 downloads from ACM Digital Library (5 Jan 2019)

18 Gina Alioto; Paul Carpenter; Christophe Avare; Marcus Leich; Adrian Cristal; Osman Unsal. RETHINK big: European Roadmap for Hardware and Networking Optimisations for Big Data. Proceedings of Design, Automation and Test in Europe Conference and Exhibition (DATE) 2017. 27/03/2017. Available on-line at: <https://doi.org/10.23919/DATE.2017.7926969>. ISBN 978-3-9815370-9-3

Type of production: Scientific paper **Format:** Scientific and technical document or report
Relevant results: CORE B conference, 6 pages

19 Rajiv Nishtala; Paul Carpenter; Xavier Martorell; Vicinius Petrucci. Hipster: Hybrid Task Manager for Latency-Critical Cloud Workloads. Proceedings of 23rd IEEE Symposium on High Performance Computer Architecture (HPCA 2017). 04/02/2017. Available on-line at: <https://doi.org/10.1109/HPCA.2017.13>. ISBN 978-1-5090-4985-1
Type of production: Scientific paper **Format:** Scientific and technical document or report
Relevant results: CORE A* conference (acceptance rate: 22.3%), 13 pages, 14 citations, HiPEAC Paper Award, 475 full text views (May 2017 to Dec 2018; 20 months) from IEEEXplore

20 Renan Fischer e Silva; Paul Carpenter. Controlling Network Latency in Mixed Hadoop Clusters: Do We Need Active Queue Management?. Proceedings of 2016 IEEE 41st Conference on Local Computer Networks (LCN). IEEE, 10/11/2016. ISBN 978-1-5090-2054-6
Type of production: Scientific paper **Format:** Scientific and technical document or report
Relevant results: CORE A conference (acceptance rate: 28%, 5 reviews), 9 pages, 8 citations, 365 full text views (May 2017 to Dec 2018) from IEEEXplore.

21 Darko Zivanovic; Milan Radulovic; German Lloret; David Zaragoza; Janko Strassburg; Paul Carpenter; Petar Radojkovic; Eduard Ayguade. Large-Memory Nodes for Energy Efficient High-Performance Computing. Proceedings of the Second International Symposium on Memory Systems, MEMSYS 2016. 06/10/2016. ISBN 978-1-4503-4305-3
Type of production: Scientific paper
Relevant results: 7 pages, 5 citations, Best Paper Award

22 Ugljesa Milic; Paul Carpenter; Alejandro Rico; Alex Ramirez. Rebalancing the Core Front-End through HPC Code Analysis. Proceedings of 2016 IEEE International Symposium on Workload Characterization (IISWC). 27/09/2016. ISBN 978-1-5090-3895-4
Type of production: Scientific paper
Relevant results: 10 pages, 2 citations

23 Victor Garcia; Alejandro Rico; Carlos Villavieja; Paul Carpenter; Nacho Navarro; Alex Ramirez. Adaptive Runtime-Assisted Block Prefetching on Chip-Multiprocessors. International Journal of Parallel Programming. pp. 1 - 21. Springer, 29/04/2016. ISSN 0885-7458
Type of production: Scientific paper **Format:** Journal
Impact source: SCOPUS **Category:** Theoretical Computer Science
Impact index in year of publication: 1.24
Position of publication: 46 **No. of journals in the cat.:** 113
Relevant results: 21 pages, 3 citations

24 Manolis Marazakis; John Goodacre; Didier Fuin; Paul Carpenter; John Thomson; Emil Matus; Antimo Bruno; Per Stenstrom; Jerome Martin; Yves Durand; Isabelle Dor. EUROSERVER: Share-Anything Scale-Out Micro-Server Design. Proceedings of the 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE). 18/03/2016. ISBN 978-3-9815370-6-2
Type of production: Scientific paper
Relevant results: CORE B conference, 6 pages, 11 citations

25 Branimir Dickov; Paul Carpenter; Miquel Pericàs; Eduard Ayguadé. Self-Tuned Software-Managed Energy Reduction in InfiniBand Links. Proceedings 2015 IEEE 21st International Conference on Parallel and Distributed Systems ICPADS 2015. 14/12/2015. Available on-line at: <http://dx.doi.org/10.1109/ICPADS.2015.87>. ISBN 978-0-7695-5785-4
Type of production: Scientific paper **Format:** Scientific and technical document or report

Impact source: SCOPUS
Category: Hardware and Architecture
Impact index in year of publication: 0.33
Position of publication: 123
No. of journals in the cat.: 139

Relevant results: 9 pages, 3 citations

26 Renan Fischer e Silva; Paul Carpenter. Exploring Interconnect Energy Savings Under East-West Traffic Pattern of MapReduce Clusters. Proceedings 2015 IEEE 40th Conference on Local Computer Networks (LCN). 26/10/2015. Available on-line at: <http://dx.doi.org/10.1109/LCN.2015.7366278>. ISBN 978-0-7695-5785-4

Type of production: Scientific paper
Format: Scientific and technical document or report
Relevant results: CORE A conference (acceptance rate: 30%, 5 reviews), one of 3 candidates for the Best Paper Award, 9 pages, 9 citations

27 Karthikeyan P. Saravanan; Paul M. Carpenter; Alex Ramirez. Exploring Multiple Sleep Modes in On/Off based Energy Efficient HPC Networks. Proceedings 2015 33rd IEEE International Conference on Computer Design (ICCD). 18/10/2015. Available on-line at: <http://dx.doi.org/10.1109/ICCD.2015.7357084>. ISBN 978-1-4673-7165-0

Type of production: Scientific paper
Format: Scientific and technical document or report
Relevant results: 8 pages, 4 citations

28 Peter Radojkovic; Paul Carpenter; Miquel Moretó; Vladimir Cakarevic; Javier Verdu; Alex Pajuelo; Francisco Cazorla; Mario Nemirovsky; Mateo Valero. Thread Assignment in Multicore/Multithreaded Processors: A Statistical Approach. IEEE Transactions on Computers. pp. 256 - 269. IEEE, 27/03/2015. Available on-line at: <http://dx.doi.org/10.1109/TC.2015.2417533>.

Type of production: Scientific paper
Format: Journal
Position of signature: 2
Degree of contribution: Author or co-author of article in journal with external admissions assessment committee
Total no. authors: 9
Corresponding author: No
Impact source: SCOPUS
Category: Theoretical Computer Science
Impact index in year of publication: 2.87
Journal in the top 25%: Yes
Position of publication: 10
No. of journals in the cat.: 118

Relevant results: Featured paper of the month for January 2016 (1 featured paper of 28 published), promoted on front page and downloadable for free for one month, with English and Chinese videos. 14 pages, 5 citations.

29 Branimir Dickov; Miquel Pericàs; Paul Carpenter; Nacho Navarro; Eduard Ayguade. Analyzing Performance Improvements and Energy Savings in Infiniband Architecture using Network Compression. 2014 IEEE 26th International Symposium on Computer Architecture and High Performance Computing. 22/10/2014. Available on-line at: <http://dx.doi.org/10.1109/SBAC-PAD.2014.27>. ISBN 978-1-4799-6904-3

Type of production: Scientific paper
Format: Scientific and technical document or report
Relevant results: 8 pages, 4 citations

30 Branimir Dickov; Miquel Pericàs; Paul Carpenter; Nacho Navarro; Eduard Ayguade. Software-Managed Power Reduction in Infiniband Links. 43rd International Conference on Parallel Processing (ICPP), 2014. pp. 311 - 320. 09/09/2014. ISBN 978-1-4799-5618-0

Type of production: Scientific paper
Relevant results: CORE A conference (acceptance rate: 36%, 4 reviews), 10 pages, 14 citations

31 Yves Durand; Paul Carpenter; Stefano Adami; Angelos Bilas; Denis Dutoit; Alexis Farcy; Georgi Gaydadjiev; John Goodacre; Manolis Katevenis; Manolis Marazakis; Emil Matus; Iakovos Mavroidis; John Thomson. EUROSERVER: Energy Efficient Node for European Micro-Servers. Euromicro Conference on Digital System Design (DSD) 2014. 27/08/2014. Available on-line at: <http://dx.doi.org/10.1109/DSD.2014.15>. ISBN 978-1-4799-5793-4

Type of production: Scientific paper
Format: Scientific and technical document or report

Relevant results: 8 pages, 35 citations

32 Karthikeyan Saravanan; Paul Carpenter; Alex Ramirez. A Performance Perspective on Energy Efficient HPC Links. Proceedings of the 28th ACM international conference on Supercomputing. pp. 313 - 322. 13/06/2014. ISBN 978-1-4503-2642-1

Type of production: Scientific paper

Impact source: SCOPUS
Category: General Computer Science
Impact index in year of publication: 1.76
Journal in the top 25%: Yes
Position of publication: 36
No. of journals in the cat.: 196

Relevant results: CORE A conference (acceptance rate: 21%, 4 reviews), 10 pages, 15 citations

33 Nikola Rajovic; Paul M. Carpenter; Isaac Gelado; Nikola Puzovic; Alex Ramirez; Mateo Valero. Supercomputing with Commodity CPUs: Are Mobile SoCs Ready for HPC?. Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis. 17/11/2013. ISBN 978-1-4503-2378-9

Type of production: Scientific paper

Relevant results: CORE A conference (acceptance rate: 20%), 12 pages, 138 citations, Best Student Paper Award

34 Karthikeyan P. Saravanan; Paul M. Carpenter; Alex Ramirez. Power/Performance Evaluation of Energy Efficient Ethernet (EEE). Proc. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2013. pp. 205 - 214. 21/04/2013. ISBN 978-1-4673-5777-7

Type of production: Scientific paper

Relevant results: CORE C conference, 10 pages, 31 citations

35 Petar Radojkovic; Paul M. Carpenter; Miquel Moretó; Alex Ramirez; Francisco J. Cazorla. Kernel Partitioning of Streaming Applications: A Statistical Approach to an NP-complete Problem. Proceedings of the 2012 45th Annual IEEE/ACM International Symposium on Microarchitecture. pp. 401 - 412. 01/12/2012. ISBN 978-0-7695-4924-8

Type of production: Scientific paper

Relevant results: CORE A conference (acceptance rate: 17%, 6 reviews), 12 pages, 4 citations, HiPEAC Paper Award

36 Paul Carpenter; Alex Ramirez; Eduard Ayguadé. The Abstract Streaming Machine: Compile-Time Performance Modelling of Stream Programs on Heterogeneous Multiprocessors. Transactions on HiPEAC. 5 - 3, Per Stenstrom, 01/01/2011. ISBN 978-3-642-19448-1

Type of production: Scientific paper
Format: Journal
Position of signature: 1
Total no. authors: 3
Corresponding author: Yes
Relevant results: 20 pages

37 Paul M. Carpenter; Alex Ramirez; Eduard Ayguade. Starsscheck: A tool to find errors in task-based parallel programs. 16th International Euro-Par Conference Ischia, Italy, August 31 - September 3, 2010 Proceedings, Part 1. pp. 2 - 13. 31/08/2010. ISBN 978-3-642-15276-4

Type of production: Scientific paper

Relevant results: CORE A conference (acceptance rate: 35%), 12 pages, 6 citations

38 Harm Munk; Eduard Ayguadé; Cédric Bastoul; Paul Carpenter; Zbigniew Chamski; Albert Cohen; Marco Cornero; Philippe Dumont; Marc Duranton; Mohammed Fellahi; Roger Ferrer; Razya Ladelszy; Menno Lindwer; Xavier Martorell; Cupertino Miranda; Dorit Nuzman; Andrea Orstein; Antoniu Pop; Sebastian Pop; Louis-Noël Pouchet; Alex Ramirez; David Rodenas; Erven Rohou; Ira Rosen; Uzi Shvadron; Konrad Trifunovic; Ayal Zaks. ACOTES Project: Advanced Compiler Technologies for Embedded Streaming. International Journal of Parallel Programming. 39 - 3, pp. 397 - 450. Bilha Mendelson, Koen Bosschere, Mateo Valero, 01/04/2010. ISSN 0885-7458

Type of production: Scientific paper **Format:** Journal
Position of signature: 4
Impact source: SJR
Impact index in year of publication: 0.554

Relevant results: 68 pages, 26 citations

39 Paul Carpenter; Alex Ramirez; Eduard Ayguade. Buffer sizing for self-timed stream programs on heterogeneous distributed memory multiprocessors. Lecture Notes in Computer Science. 5952, pp. 96 - 110. 25/01/2010. ISBN 978-3-642-11514-1
Type of production: Scientific paper **Format:** Journal
Impact source: SCOPUS **Category:** General Computer Science
Impact index in year of publication: 0.49
Position of publication: 91 **No. of journals in the cat.:** 136

Relevant results: 15 pages, 6 citations

40 Paul Carpenter; Alex Ramirez; Eduard Ayguade. Mapping stream programs onto heterogeneous multiprocessor systems. Proceedings of the 2009 international conference on Compilers, architecture, and synthesis for embedded systems. pp. 57 - 66. 11/10/2009.
Type of production: Scientific paper
Relevant results: CORE A conference (acceptance rate: 43%, 4 reviews), 10 pages, 34 citations

41 Paul Carpenter; Alex Ramirez; Eduard Ayguadé. The Abstract Streaming Machine: Compile-Time Performance Modeling of Stream Programs on Heterogeneous Processors. Lectures Notes in Computer Science. 5657, Springer, 21/07/2009.
Type of production: Scientific paper
Position of signature: 1
Total no. authors: 3 **Corresponding author:** Yes
Impact source: SJR
Impact index in year of publication: 0.342

Relevant results: 11 pages, 6 citations

42 Paul Carpenter; Alex Ramirez; Eduard Ayguade. The Abstract Streaming Machine. HiPEAC ACACES 2008 Summer School Poster Abstracts. Academic Press. pp. 305 - 308. 16/07/2008. ISBN 978 90 382 1288 3
Type of production: Scientific paper
Position of signature: 1
Relevant results: 4 pages

43 Paul Carpenter; David Rodenas; Xavier Martorell; Alex Ramirez; Eduard Ayguadé. A Streaming Machine Description and Programming Model. Lecture Notes in Computer Science. 4599, pp. 107 - 116. Springer, 07/2007.
Type of production: Scientific paper
Impact source: SJR
Impact index in year of publication: 0.311

Relevant results: 10 pages, 24 citations

44 Paul Carpenter; Guy Lonsdale. Technical Research Priorities: Programming Environment. In ETP4HPC Strategic Research Agenda 2015 Update. 16/12/2015.
Type of production: Book chapter **Format:** Scientific and technical document or report

45 Paul Carpenter; Guy Lonsdale. Technical Research Priorities: Programming Environment. In ETP4HPC Strategic Research Agenda. 05/2013.
Type of production: Book chapter

46 Utz-Uwe Haus; Erwin Laure; Sai Narasimhamurthy; Estela Suarez. Heterogeneous High Performance Computing. ETP4HPC, 15/02/2022.
Type of production: Scientific-technical report

47 Olivier Aumage; Paul Carpenter; Siegfried Benkner. Task-Based Performance Portability in HPC. ETP4HPC, 05/10/2021.
Type of production: Scientific-technical report

48 Petar Radojkovic; Paul Carpenter; Pouya Esmaili-Dokht; Rémy Cimadomo; Charles Henri-Pierre; Abu Sebastian; Paolo Amato. Processing in Memory: The Tipping Point. ETP4HPC, 29/07/2021.
Type of production: Scientific-technical report **Format:** Scientific and technical document or report

49 Theo Ungerer; Paul Carpenter. EuroLab-4-HPC Long-Term Vision on High-Performance Computing. 31/07/2017. Available on-line at: <https://www.eurolab4hpc.eu/roadmap/>.
Type of production: Scientific-technical report **Format:** Book
Relevant results: 147 downloads (September to October 2017; 2 months; figures as of project review)

50 Theo Ungerer; Paul Carpenter; Mike Knebel. Preliminary EuroLab-4-HPC Roadmap. 31/08/2016.
Type of production: Scientific-technical report **Format:** Scientific and technical document or report

51 Paul Carpenter; David Rodenas; Xavier Martorell; Alex Ramirez; Eduard Ayguadé. Code generation for streaming applications based on an abstract machine description. 04/2007.
Type of production: Scientific-technical report
Position of signature: 1

52 Felippe Vieira Zacarias; Paul Carpenter; Vinicius Petrucci. Dynamic memory provisioning of disaggregated HPC systems. MTSA'23: Workshop on Memory Technologies, Systems, and Applications. 13/11/2023.

53 Omar Shaaban; Jimmy Aguilar Mena; Vicenç Beltran; Paul Carpenter; Eduard Ayguadé; Jesus Labarta. Automatic aggregation of subtask accesses for nested OpenMP-style tasks. EEE 34th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2022). IEEE, 02/11/2022.

54 Jimmy Aguilar Mena; Omar Shaaban; Vicenç Beltran; Paul Carpenter; Eduard Ayguadé; Jesus Labarta. OmpSs-2@Cluster: Distributed memory execution of nested OpenMP-style tasks. European Conference on Parallel Processing, Euro-Par 2022. 29/08/2022.

55 Jimmy Aguilar Mena; Omar Shaaban; Victor Lopez; Marta Garcia; Paul Carpenter; Eduard Ayguadé; Jesus Labarta. Transparent load balancing of MPI programs using OmpSs-2@Cluster and DLB. 51st International Conference on Parallel Processing. 22/08/2022.

56 Felippe Vieira Zacarias; Vinicius Petrucci; Paul Carpenter. Improving HPC System Throughput and Response Time using Memory Disaggregation. IEEE International Conference on Parallel and Distributed Systems (ICPADS 2021). IEEE, 14/12/2021.

57 Felippe Vieira Zacarias; Vinicius Petrucci; Paul Carpenter. Memory Demands in Disaggregated HPC: How Accurate Do We Need to Be. International Workshop on Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems (PMBS 2021). IEEE, 15/11/2021.

Relevant results: Best short paper award

58 Felippe Vieira Zacarias; Vinicius Petrucci; Rajiv Nishtala; Paul Carpenter; Daniel Mosse. Intelligent Colocation of Server Workloads. Journal of Parallel and Distributed Computing (JPDC).151, pp. 125 - 137. 01/05/2021.

59 Isaac Boixaderas; Javier Bartolome; Paul Carpenter; David Vicente; Petar Radojkovic; Sergi More; Marc Casas; Eduard Ayguade. Cost-Aware Prediction of Uncorrected DRAM Errors in the Field. International Conference for High Performance Computing, Networking, Storage, and Analysis, SC'20. 16/11/2020.

60 Felippe Vieira; Rajiv Nishtala; Paul Carpenter. Contention-aware Application Performance Prediction for Disaggregated Memory Systems. Computing Frontiers 2020. 11/05/2020.

61 Behzad Salami; K. Parasyris; A. Cristal; O. Unsal; X. Martorell; P. Carpenter; R. De La Cruz; L. Bautista; D. Jimenez; C. Alvarez; S. Nabavi; S. Madonar; M. Pericàs; P. Trancoso; M. Abduljabbar; J. Chen; P. N. Soomro; M. Manivannan; M. Berge; S. Krupop; F. Klawonn; Al Mekhlafi; S. May; T. Becker; G. Gaydadjiev; D. Odman; H. Salomonsson; D. Dubhashi; O. Port; Y. Etsion; Le Quoc Do; C. Fetzer; M. Kaiser; N. Kucza; J. Hagemeyer; R. Griessl; L. Tigges; K. Mika; A. Huffmeier; Th. Jungeblut; M. Pasin; V. Schiavoni; I. Rocha; C. Göttel; P. Felber. LEGaTO: Low-Energy, Secure, and Resilient Toolset for Heterogeneous Computing. Design, Automation and Test in Europe Conference and Exhibition (DATE 2020). 09/03/2020.

62 Felippe Zacarias; Vinicius Petrucci; Rajiv Nishtala; Paul Carpenter; Daniel Mosse. Intelligent Colocation of Workloads for Enhanced Server Efficiency. 31st International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD). 15/10/2019.

63 Darko Zivanovic; Pouya Esmaili-Dokht; Sergi More; Javier Bartolome; Paul Carpenter; Petar Radojkovic; Eduard Ayguade. DRAM Errors in the Field: A Statistical Approach. MEMSYS '19: Proceedings of the International Symposium on Memory Systems. 30/09/2019.

64 Milan Radulovic; Rommel Sanchez Verdejo; Paul Carpenter; Petar Radojkovic; Bruce Jacob; Eduard Ayguade. PROFET: Modeling System Performance and Energy Without Simulating the CPU. ACM SIGMETRICS / IFIP Performance. 24/06/2019.

65 Luis Garrido; Rajiv Nishtala; Paul Carpenter. Continuous-Action Reinforcement Learning for Memory Allocation in Virtualized Servers. 15th Workshop on Virtualization in High-Performance Cloud Computing (VHPC'20). 20/06/2019.

66 Rajiv Nishtala; Paul Carpenter. SmarTmem: Intelligent Management of Transcendent Memory in a Virtualized Server. RADR Workshop 2019. 24/05/2019.

Works submitted to national or international conferences

1 **Title of the work:** Exascale System Software and Programming Models
Name of the conference: SIAM Conference on Computational Science and Engineering (CSE23)
Date of event: 27/01/2023
Organising entity: Society for Industrial and Applied Mathematics
Paul Carpenter.

2 **Title of the work:** Composability at the Boundary between HPC and Cloud
Name of the conference: First Workshop on Composable Systems (COMPSYS)
Date of event: 03/06/2022

Paul Carpenter.

3 **Title of the work:** HPC job scheduling to exploit disaggregated memory
Name of the conference: Software & Hardware Co-Design Workshop 2021
Date of event: 10/06/2021
Organising entity: Huawei European Research Institute (ERI), Huawei Cambridge Research Center
Paul Carpenter.

4 **Title of the work:** Runtime Systems & hardware acceleration for HPC
Name of the conference: Convergence of Big-Data Analytics, Cloud, and High-performance Computing with EVOLVE
Corresponding author: Yes
City of event: Bilbao, Basque Country, Spain
Date of event: 30/10/2019
End date: 30/10/2019
Paul Carpenter. Available on-line at: <https://www.hipeac.net/csw/2019/bilbao/#/schedule/sessions/7762/>.

5 **Title of the work:** Applications on the FPGA-based EuroEXA prototype: lessons learnt and progress so far
Name of the conference: 1st International Workshop on Reconfigurable High Performance Computing (ReHPC'2019)
Corresponding author: Yes
City of event: Barcelona, Spain
Date of event: 13/09/2019
End date: 13/09/2019
Paul Carpenter.

6 **Title of the work:** Keynote talk: The path to portable and malleable HPC applications
Name of the conference: 2019 International Conference on High Performance Computing & Simulation (HPCS 2019)
Type of event: Conference
Type of participation: Participatory - invited/keynote talk
Corresponding author: Yes
City of event: Dublin, Ireland
Date of event: 15/07/2019
End date: 19/07/2019
Paul Carpenter.

7 **Title of the work:** The greatest challenges and opportunities inpost-exascale programming
Name of the conference: 3rd Workshop on HPC Computing in a Post Moore´s Law World (HCPM) 2019
Corresponding author: Yes
City of event: Frankfurt, Germany
Date of event: 20/06/2019
End date: 20/06/2019
Paul Carpenter.

8 **Title of the work:** Extreme Heterogeneity in the EuroEXA projec
Name of the conference: Salishan Conference on High-Speed Computing
Type of event: Conference
Type of participation: Participatory - invited/keynote talk **Reasons for participation:** Upon invitation
Corresponding author: Yes

City of event: Gleneden Beach, Oregon, United States of America
Date of event: 24/04/2019
Organising entity: Lawrence Livermore, Los Alamos, and Sandia National Laboratories
Paul Carpenter.

9 **Title of the work:** Reconfigurable Computing in the EuroEXA Project
Name of the conference: 13th HiPEAC Workshop on Reconfigurable Computing (WRC'2019)
Type of event: Workshop
Type of participation: Participatory - invited/keynote **Reasons for participation:** Upon invitation talk
Corresponding author: Yes
Date of event: 21/01/2019
Paul Carpenter.

10 **Title of the work:** ExaNoDe, including Hardware/ Technology and Systems Software
Name of the conference: The Projects ExaNeSt, ECOSCALE, ExaNoDe, and the links among them and with EuroEXA
Type of event: Workshop
City of event: Daresbury, United Kingdom
Date of event: 07/11/2018
Denis Dutoit; Paul Carpenter.

11 **Title of the work:** EuroEXA & ExaNoDe: Co-designed Applications and Software Stack
Name of the conference: 7th Annual Spain Conference
Date of event: 21/09/2018
Organising entity: HPC-AI Advisory Council
Paul Carpenter.

12 **Title of the work:** Task-based parallelism for efficient cluster programming
Name of the conference: Towards Exascale HPC systems: Co-design and Technology development within the EuroEXA, ExaNeSt, ExaNoDe and EcoScale projects
City of event: Ljubljana, Slovenia
Date of event: 31/05/2018
Organising entity: EXDCI
Babis Chalios; Paul Carpenter.

13 **Title of the work:** EuroEXA co-design, demonstration and evaluation using a rich set of exascale-class applications
Name of the conference: ExascaleHPC Workshop
Type of event: Workshop
Type of participation: Participatory - oral communication
Corresponding author: Yes
City of event: Manchester, United Kingdom
Date of event: 23/01/2018
With external admission assessment committee: Yes
Paul Carpenter.

14 **Title of the work:** FETHPC Highlight: OmpSs (ExaNode)
Name of the conference: EXDCI Workshop
Type of participation: Participatory - oral communication
Corresponding author: Yes

City of event: Barcelona, Spain
Date of event: 15/05/2017
With external admission assessment committee: Yes
Paul Carpenter; Babis Chalios; Jimmy Aguilar Mena.

15 **Title of the work:** Workshop Software for HPC and data centers: the role of open source, convergence, trends. Panel discussion member
Name of the conference: HiPEAC Computing Systems Week
Type of participation: Participatory - oral communication
City of event: Zagreb, Croatia
Date of event: 28/04/2017

16 **Title of the work:** ExaNoDe European Exascale Processor & Memory Node Design
Name of the conference: Advances in Heterogeneous HPC
Type of event: Workshop
Type of participation: Participatory - invited/keynote talk
Corresponding author: Yes
City of event: Zagreb, Croatia
Date of event: 27/04/2017
End date: 27/04/2017
Paul Carpenter; Denis Dutoit.

17 **Title of the work:** RETHINKing big data hardware: A Roadmap for European Industry
Name of the conference: Barcelona Big Data Congress 2016
Type of participation: Participatory - oral communication
Corresponding author: Yes
City of event: Barcelona,
Date of event: 05/10/2016
With external admission assessment committee: Yes
Paul Carpenter.

18 **Title of the work:** ExaNoDe European Exascale Processor & Memory Node Design
Name of the conference: ISC'16 Workshop on International Cooperation
Type of participation: Participatory - oral communication
Corresponding author: Yes
City of event: Frankfurt, Germany
Date of event: 03/08/2016
Paul Carpenter.

19 **Title of the work:** Runtime Estimation of Performance--Power in CMPs under QoS constraints
Name of the conference: 3rd Doctoral Symposium
Type of participation: Participatory - others
City of event: Barcelona, Spain
Date of event: 06/05/2016
Publication in conference proceedings: Yes
Rajiv Nishtala; Xavier Martorell; Paul Carpenter. "Book of Abstracts, 3rd BSC International Doctoral Symposium". 09/2016. Available on-line at: <https://www.bsc.es/education/predoctoral-phd/doctoral-symposium/3rd-international-bsc-doctoral-symposium-2016>.

20 **Title of the work:** State of Preliminary Eurolab-4-HPC Roadmap
Name of the conference: HiPEAC Computing Systems Week
Type of participation: Participatory - oral communication
City of event: Porto, Portugal
Date of event: 20/04/2016
Theo Ungerer; Paul Carpenter.

21 **Title of the work:** ALYA Multi-Physics System on GPUs: Offloading Large-Scale Computational Mechanics Problems
Name of the conference: GPU Technology Conference (GTC)
Type of participation: Participatory - others
City of event: San Jose, CA, United States of America
Date of event: 04/04/2016
End date: 07/04/2016
Organising entity: Nvidia
With external admission assessment committee: Yes
Vishal Mehta; Paul Carpenter.

22 **Title of the work:** Building a globally competitive HPC technology provision value chain in Europe
Name of the conference: Big Data Value Association Summit
Type of participation: Participatory - oral communication
City of event: Madrid, Spain
Date of event: 18/06/2015
Marcin Ostacz; Paul Carpenter.

23 **Title of the work:** Exploiting CUDA Dynamic Parallelism for Low-Power ARM-Based Prototypes
Name of the conference: GPU Technology Conference (GTC)
Type of participation: Participatory - others
City of event: San Jose, CA, United States of America
Date of event: 17/03/2015
End date: 20/03/2015
Organising entity: Nvidia
Vishal Mehta; Paul Carpenter.

24 **Title of the work:** Adaptive Runtime-Assisted Block Prefetching on Chip-Multiprocessors.
Name of the conference: Third International Workshop on On-chip memory hierarchies and interconnects: organization, management and implementation, 2014
Type of participation: Participatory - others
City of event: Porto, Portugal
Date of event: 25/08/2014
End date: 25/08/2014
Publication in conference proceedings: Yes
Victor Garcia; Alejandro Rico; Carlos Villavieja; Paul Carpenter; Alex Ramirez; Nacho Navarro. "Euro-Par 2014: Parallel Processing Workshops". ISSN 0302-9743, ISBN 978-3-319-14312-5

25 **Title of the work:** MONT-BLANC: European Scalable and Power Efficient HPC Platform Based on Low-Power Embedded Technology
Name of the conference: Exascale Technologies & Innovation in HPC for Climate Models - 3rd HPC Workshop
Type of participation: Participatory - oral communication
Corresponding author: Yes

City of event: Hamburg, Germany
Date of event: 17/03/2014
Paul Carpenter.

26 **Title of the work:** Position of Mont-Blanc 2 Project
Name of the conference: EU Workshop on Next Generation Computing Systems: Components and Architectures for a Scalable Market
Corresponding author: Yes
City of event: Brussels, Belgium
Date of event: 10/12/2013
Paul Carpenter.

27 **Title of the work:** The Mont-Blanc Project: Are Mobile Processors Ready for HPC?
Name of the conference: Fourth AICS International Symposium
Type of participation: Participatory - invited/keynote talk
Corresponding author: Yes
City of event: Kobe, Japan
Date of event: 02/12/2013
Paul Carpenter; Nikola Rajovic; Nikola Puzovic; Alex Ramirez.

28 **Title of the work:** European Scalable and Power Efficient HPC Platform Based on Low-Power Embedded Technology
Name of the conference: ISCA 2013 EU-FP7 Workshop: Synopsis of FP7 Computer Systems and Transitioning to Horizon 2020
Type of participation: Participatory - invited/keynote talk
City of event: Tel Aviv, Israel
Date of event: 23/06/2013
Alex Ramirez; Paul Carpenter.

29 **Title of the work:** Experiences with Mobile Processors for Energy Efficient HPC. Speaker and panel discussion member.
Name of the conference: Low Energy Application Parallelism (LEAP) Conference
Type of participation: Participatory - invited/keynote talk
City of event: London, United Kingdom
Date of event: 21/05/2013
Alex Ramirez; Nikola Rajovic; Alejandro Rico; James Vipond; Paul Carpenter; Nikola Puzovic.

30 **Title of the work:** Embedding High Performance Computing: A supercomputer in your pocket or ultra low power exaflop design? Panel discussion member
Name of the conference: Design, Automation & Test in Europe (DATE), 2013
Type of participation: Participatory - oral communication
City of event: Grenoble, France
Date of event: 22/03/2013

31 **Title of the work:** Experiences with Mobile Processors for Energy Efficient HPC
Name of the conference: Design, Automation & Test in Europe (DATE), 2013
Type of participation: Participatory - invited/keynote talk
City of event: Grenoble, France
Date of event: 20/03/2013
Alex Ramirez; Nikola Rajovic; Alejandro Rico; James Vipond; Nikola Puzovic; Paul Carpenter.

32 **Title of the work:** The Next Generation Supercomputer
Name of the conference: IS-ENES workshop on HPC for Climate Models
Type of participation: Participatory - invited/keynote talk
Corresponding author: Yes
City of event: Toulouse, France
Date of event: 30/01/2013
Paul Carpenter.

33 **Title of the work:** The Abstract Streaming Machine: Compile-Time Performance Modelling of Stream Programs on Heterogeneous Multiprocessors
Name of the conference: SAMOS Workshop - International Workshop on Systems, Architectures, Modeling, and Simulation (Best paper award)
Type of participation: Participatory - oral communication
City of event: Samos, Greece
Date of event: 20/07/2009
End date: 23/07/2009
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Paul Carpenter; Alex Ramirez; Eduard Ayguadé. En: Lecture Notes in Computer Science. 5657, Koen Bertels, Nikitas Dimopoulos, Cristina Silvano, Stephan Wong, ISBN 978-3-642-03137-3

34 **Title of the work:** A Streaming Machine Description and Programming Model
Name of the conference: VII International Workshop on Systems, Architectures, Modeling, and Simulation (SAMOS Workshop VII)
Geographical area: European Union
Type of participation: Participatory - oral communication
City of event: Samos, Greece
Date of event: 16/07/2007
End date: 19/07/2007
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Paul Carpenter; David Rodenas; Xavier Martorell; Alex Ramirez; Eduard Ayguadé. En: Lecture Notes in Computer Science Vol 4599. pp. 107 - 116. Stamatis Vassiliadis, Mladen Berekovic, Timo D. Hämäläinen, ISBN 978-3-540-73622-6

35 **Title of the work:** Abstract Streaming Machine for Compiler Optimizations
Name of the conference: Third International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES 2007)
Type of participation: 'Participatory - poster
City of event: L'Aquila, Italy
Date of event: 2007
With external admission assessment committee: Yes
Paul Carpenter; Alex Ramirez; Eduard Ayguadé.

36 **Title of the work:** Audio decompression using 32-bit RISC CPU versus traditional DSP
Name of the conference: Silicon for Audio - AES 16th UK Conference
Type of event: Conference
Type of participation: Participatory - others
Date of event: 09/04/2001
End date: 10/04/2001
Publication in conference proceedings: Yes

Marc Bringmann; Paul Carpenter; John Graley. "Audio Engineering Society 16th UK Conference". En: Proceedings of the AES 16th UK Conference: Silicon for Audio.

Other dissemination activities

1 **Title of the work:** Task-based programming with OmpSs-2
Name of the event: 2023 ACM Europe Summer School on “HPC Computer Architectures for AI and Dedicated Applications
City of event: Barcelona,
Date of event: 04/07/2023
Xavier Martorell; Paul Carpenter.

2 **Title of the work:** Core- and Node-level malleability using OmpSs-2@Cluster
Name of the event: DEEP-SEA seminar
Date of event: 17/03/2023
Paul Carpenter.

3 **Title of the work:** Task-Based Performance Portability in HPC
Name of the event: ETP4HPC webinar
Date of event: 18/03/2022
Organising entity: ETP4HPC
Olivier Aumage; Paul Carpenter.

4 **Title of the work:** Programming environment: State of the Art and Future Directions
Name of the event: ETP4HPC Webinar
Date of event: 10/02/2022
Paul Carpenter.

5 **Title of the work:** Cost-Aware Prediction of Uncorrected DRAM Errorsin the Field
Name of the event: EuroEXA Workshop at HiPEAC Computing Systems Week
Type of event: Conferences given
City of event: Virtual,
Date of event: 25/02/2021
Organising entity: HiPEAC
Paul Carpenter.

6 **Title of the work:** Panel: When one size doesn't fit all: programming models in the post-Moore era
Name of the event: Fifth International IEEE Workshop on Extreme Scale Programming Models and Middleware
Type of event: Conferences given
City of event: Atlanta, Georgia, United States of America
Date of event: 11/11/2020
Nectarios Koziris; Paul Carpenter; Tarek El-Ghazawi; Jeff Hammond; Dimitrios Nikolopoulos; Thomas Stirling.

7 **Title of the work:** Eurolab4HPC: Making Europe Excel in HPC Technology
Name of the event: PRACE booth at SC'19
Corresponding author: Yes
City of event: Denver, United States of America
Date of event: 20/11/2019

Organising entity: PRACE
Paul Carpenter.

8 **Title of the work:** Presenter and panel member
Name of the event: EXDCI BoF at SC 2018: Consolidating the European Exascale Effort
City of event: Dallas, United States of America
Date of event: 14/11/2018
Organising entity: EXDCI2
Paul Carpenter. "EuroExa".

9 **Title of the work:** The Eurolab4HPC Vision (dissemination of Eurolab4HPC Vision document)
Name of the event: EuroLab-4-HPC Workshop, HPC Summit 2018
Type of event: Conferences given
City of event: Ljubljana, Slovenia
Date of event: 31/05/2018
Organising entity: EXDCI
Paul Carpenter; Theo Ungerer.

10 **Title of the work:** Heidelberg Laureate Forum 2014
Name of the event: BSC Severo Ochoa Christmas Lecture
Type of event: Conferences given
City of event: Barcelona, Spain
Date of event: 16/12/2016

11 **Title of the work:** Promotion video for EUROSERVER Workshop at HiPEAC Conference
Date of event: 05/12/2016
Paul Carpenter.

12 **Title of the work:** ExaNoDe video interview for Primeur Magazine
Name of the event: ISC 2016
Type of event: Media interviews
City of event: Frankfurt, Germany
Date of event: 23/06/2016
Organising entity: Primeur Magazine
Paul Carpenter. Available on-line at: <http://primeurmagazine.com/weekly/AE-PR-09-16-33.html>.

13 **Title of the work:** ARM technology video interview for ARM Annual Partner Meeting
City of event: Frankfurt, Germany
Date of event: 22/06/2016
Paul Carpenter.

14 **Title of the work:** Extreme Value Theory: Solving intractable computer science problems. Dissemination video for Extreme Value Theory. Coauthor and narrator.
Date of event: 12/2015
Available on-line at: <https://www.youtube.com/watch?v=Zaq2g_bVD6s>.

15 **Title of the work:** Euroserver project booth
Name of the event: ARTEMISIA Co-Summit 2015
Type of event: Fairs and exhibitions
City of event: Berlin, Germany
Date of event: 10/03/2015

Organising entity: ARTEMIS Industry Association

16 **Title of the work:** Press Release: Europe invests realising next-generation green computing for micro-servers and scalable compute
Date of event: 28/03/2014

17 **Title of the work:** The Mont-Blanc Approach Towards Exascale; Leader discussion section on Advanced Architecture.
Name of the event: BUX Bull User Group
Type of event: Conferences given
City of event: Warwick, United Kingdom
Date of event: 05/09/2012
Alex Ramirez; Paul Carpenter (presenter).

18 **Title of the work:** Alya Red: A computational heart. Dissemination video for Alya Red simulation of a human heart. Narrator. Winner of International Science & Engineering Visualization Challenge (video) by National Science Foundation and Science Magazine.
Date of event: 09/2012
Available on-line at: <https://www.youtube.com/watch?v=hiKgDOXlPfk>.

19 **Title of the work:** Optimizing Digital Video Codecs in ARM Cores
Date of event: 20/09/2001
Alan Lewis; Paul Carpenter. "EE Times". Available on-line at: <https://www.eetimes.com/document.asp?doc_id=1225211>.

20 **Title of the work:** An Optimised Software Solution for an ARM Powered MP3 Decoder
Date of event: 27/10/2000
Barney Wragg; Paul Carpenter. Available on-line at: <https://www.mp3-tech.org/programmer/docs/mp3_wp.pdf>.

R&D management and participation in scientific committees

Scientific, technical and/or assessment committees

1 **Committee title:** CCGrid 2022 Program Committee member
Start-End date: 2021 - 2022

2 **Committee title:** HiPEAC Collaboration Grants reviewer
Start-End date: 03/12/2021 - 18/12/2021

3 **Committee title:** IEEE International Symposium on Network Computing and Applications (NCA 2020) Program Committee
Start-End date: 31/07/2020 - 23/11/2020

4 **Committee title:** Diego Braga PhD proposal committee
Affiliation entity: University of Pittsburgh
City affiliation entity: Pittsburg,
Start-End date: 13/08/2020 - 13/08/2020

5 **Committee title:** Review Master thesis Karl Andreas Holberg and Alf Martin Holberg
Affiliation entity: Norwegian University of Science and Technology (NTNU) **Type of entity:** University
City affiliation entity: Trondheim, Norway
Start-End date: 25/09/2019 - 08/11/2019

6 **Committee title:** International Symposium on Advanced Parallel Processing Technology, APPT 2019: Program Committee member
Start-End date: 27/02/2019 - 15/08/2019

7 **Committee title:** Comité Evaluador de propuestas de proyectos en I+D+i de la Convocatoria CEPRA XIV *
Affiliation entity: Corporación Ecuatoriana para el Desarrollo de la Investigación y la Academia (CEDIA) **Type of entity:** Public Research Body
City affiliation entity: Cuenca, Ecuador
Start-End date: 07/11/2019 - 2019

8 **Committee title:** Evaluation of Proyectos de Investigación Científica y Tecnológica (PICT): Middlewares Energéticamente Eficientes para Computación Distribuida Orientada a Servicios a través de Dispositivos Móviles
Affiliation entity: Agencia Nacional de Promoción Científica y Tecnológica de Argentina **Type of entity:** State agency
Start-End date: 04/01/2018 - 25/01/2018

9 **Committee title:** Submission Chair and Program Committee member PACT 2018, International Conference on Parallel Architectures and Compilation Techniques (CORE A)
Start-End date: 2018 - 2018

10 **Committee title:** Leader of Working Group on HPC application evolution and requirements
Affiliation entity: EuroLab-4-HPC
Start-End date: 01/09/2015 - 31/08/2017

11 **Committee title:** Workshop on Parallel Software Tools and Tool Infrastructures (PSTI 2017), Program Committee
Start-End date: 15/04/2017 - 15/05/2017

12 **Committee title:** Member of EESI2 working group on energy efficiency. The main goals of the second European Exascale Software Initiative (EESI2) were to elaborate an evolutive European vision and roadmap and to propose recommendations to address the challenges of Extreme Data and Extreme Computing on the new generation of Exascale computers expected in 2020.
Start date: 20/06/2014

13 **Committee title:** ?European Technology Platform for High Performance Computing (ETP4HPC) Strategic Research Agenda Co-chair Working Group on Programming Models. ETP4HPC is the industry-led forum that, in dialog with the European Commission, defines the European HPC technology research priorities to achieve EU growth, competitiveness and sustainability
Geographical area: European Union
Affiliation entity: European Technology Platform for High-Performance Computing (ETP4HPC) **Type of entity:** Associations and Groups
City affiliation entity: Amsterdam, Noord-Holland, Holland
Start date: 25/05/2012

14 **Committee title:** IEEE IPDPS 2013 Program Committee
Geographical area: Non EU International

Organization of R&D activities

1 **Title of the activity:** Challenges and Opportunities in Academic HPC Systems Researchin 2030
Type of activity: Birds of a Feather session **Geographical area:** Non EU International
City convening entity: Denver, United States of America
Start-End date: 20/11/2019 - 20/11/2019

2 **Title of the activity:** Application Scaling and Porting on an FPGA-based Supercomputer in the EuroEXA Project, PASC Mini-symposium
City of event: Zurich, Switzerland
Type of participation: Organiser
Start-End date: 12/06/2019 - 14/06/2019

3 **Title of the activity:** Thematic Session: EuroLab4HPC Open Source Software and Hardware
City of event: Heraklion, Greece
Type of participation: Organiser
Start-End date: 31/10/2018 - 31/10/2018

4 **Title of the activity:** Thematic Session: EuroLab4HPC Session on Accelerators
Type of activity: Workshop
City of event: Heraklion, Greece
Type of participation: Organiser
Start-End date: 30/10/2018 - 30/10/2018

5 **Title of the activity:** Exascale computing workshop: experiences and best practices for porting applications to emerging HPC architectures and platforms
Type of activity: Workshop
City of event: Vicenza, Italy
Type of participation: Organiser
Start-End date: 08/10/2018 - 09/10/2018

6 **Title of the activity:** EuroEXA WP2/WP3 Workshop
Type of activity: Workshop **Geographical area:** European Union
City convening entity: Stuttgart, Germany
Start-End date: 27/10/2017 - 27/10/2017

7 **Title of the activity:** DTHPC: Workshop on Disruptive Technologies in High-Performance Computing in the Next Decade
Type of activity: Workshop
City of event: Stockholm, Sweden
Convening entity: HiPEAC
Type of participation: Organiser
Start-End date: 23/01/2017 - 25/01/2017

8 **Title of the activity:** EUROSERVER: Green Data Centers / Microserver: System architecture, Software tools
Type of activity: Workshop

City of event: Stockholm, Sweden
Convening entity: HiPEAC **Type of entity:** Associations and Groups
Type of participation: Organiser
Start-End date: 23/01/2017 - 25/01/2017

9 **Title of the activity:** EuroLab-4-HPC: Fostering Excellence in HPC System Research. Co-organiser.
Type of activity: Workshop
City of event: Milan, Italy
Type of participation: Organiser
Start-End date: 21/09/2015 - 21/09/2015 **Duration:** 1 day

National and international forums and committees

1 **Name of the forum:** 2020 International Conference on High Performance Computing & Simulation (HPCS 2020)
Professional category: General Co-Chair
Start-End date: 22/02/2020 - 27/03/2021

2 **Name of the forum:** HPBench: 7th Special Session on High Performance Computing Benchmarking and Optimization Program Committee Member
Start-End date: 27/05/2020 - 29/01/2021

3 **Name of the forum:** Paul Caheny PhD predefence (President)
Organising entity: Universitat Politècnica de Catalunya
Start date: 20/07/2020

4 **Name of the forum:** Dimitrios Chasapis PhD predefence (vocal)
Organising entity: Universitat Politècnica de Catalunya
Start date: 22/11/2018

5 **Name of the forum:** Thomas Grass PhD defence (secretari)
Organising entity: Universitat Politècnica de Catalunya
Start date: 09/10/2017

6 **Name of the forum:** Victor Garcia PhD predefence (vocal)
Organising entity: Universitat Politècnica de Catalunya **Type of entity:** University
Start date: 08/06/2017

7 **Name of the forum:** Thomas Grass PhD predefence (vocal)
Organising entity: Universitat Politècnica de Catalunya **Type of entity:** University
Start date: 06/06/2017

8 **Name of the forum:** Milan Pavlovic PhD predefence (Secretari)
Organising entity: Universitat Politècnica de Catalunya **Type of entity:** University
Start date: 02/10/2015

9 **Name of the forum:** Vinoth Elangovan PhD predefence (vocal)
Organising entity: Universitat Politècnica de Catalunya **Type of entity:** University
Start date: 13/11/2014

10 **Name of the forum:** Tassadaq Hussain PhD predefence (President)
Organising entity: Universitat Politècnica de Catalunya **Type of entity:** University
Start date: 03/10/2014

Evaluation and revision of R&D projects and articles

1 **Performed tasks:** Program Committee member IEEE International Symposium on Network Computing and Applications (NCA 2018, 2019 and 2020) (CORE A)
Type of activity: Review of articles in scientific or technological journals
Geographical area: Non EU International
Start-End date: 01/08/2018 - 15/09/2020

2 **Performed tasks:** EuroExaScale Workshop 2020 Program Committee member
Start-End date: 2019 - 20/01/2020

3 **Performed tasks:** Reviewer for Concurso Ecuatoriano de proyectos de I+D+i en su XIV convocatori
Entity where activity was carried out: Corporación Ecuatoriana para el Desarrollo de la Investigación y la Academia **Type of entity:** State agency
City of entity: Quito, Ecuador
Start-End date: 2019 - 2019

4 **Performed tasks:** Reviewer for HiPEAC Vision 2019
Type of activity: Acknowledged reviewer
Start-End date: 16/11/2018 - 30/11/2018

5 **Performed tasks:** Reviewer for IEEE Access
Start-End date: 25/07/2018 - 30/07/2018

6 **Performed tasks:** Program Committee member Euro-Par 2024
Start date: 2024

7 **Performed tasks:** Program committee member ALCHEMY Track of ICCS2019
Start date: 31/10/2018

8 **Performed tasks:** Reviewer IEEE Transactions on Computers (CiteScore 3.42)
Start date: 05/2017

9 **Performed tasks:** Member of PSTI Workshop 2017 Program Committee
Start date: 2017

10 **Performed tasks:** Member of IPDPS 2013 Program Committee (CORE A)
Start date: 2013

11 **Performed tasks:** Reviewer for Scientific Programming (2017), Microprocessors and Microsystems (2011, 2016), IEEE Transactions on Parallel and Distributed Systems (2012, 2013), ICCD 2012, IEEE IPDPS 2013 PhD Forum, International Journal of Parallel Programming (2011, 2012) and IEEE Access (2014). Reviewed papers for IPDPS 2011, Euro-Par 2012, TACO 2012 and Euro-Par 2013.

Other achievements

Stays in public or private R&D centres

1 **Entity:** Berkeley Design Technology, Inc. (BDTI)
City of entity: Berkeley, United States of America
Start-End date: 25/07/2005 - 28/10/2005 **Duration:** 3 months
Goals of the stay: Independent Consultant
Provable tasks: External consultant: performance analysis of multimedia codec and micro-benchmarks on ARM11 and ARM Cortex-A8 processor. Delivered two-day training course to BDTI engineers.

2 **Entity:** ARM Limited
City of entity: Cambridge, East Anglia, United Kingdom
Start-End date: 16/06/2003 - 08/04/2005 **Duration:** 1 year - 10 months
Goals of the stay: Independent Consultant
Provable tasks: External consultant to the small team (5 people) in the ARM Research Group (corporate headquarters in Cambridge, UK) that designed the ARM Advanced SIMD / NEON vector ISA. Inventor on one related worldwide patent. Author of NEON software training material (presentation and document "NEON Code Examples", RDB01-GENC-003057). Advanced SIMD was introduced in ARM Cortex-A8 (2005) and the design has changed little as of 2015. Advanced SIMD is mandatory in the latest ARM Architecture (ARMv8-A), and in 64-bit mode it is the only support for SIMD.

3 **Entity:** Cirrus Logic
City of entity: Denver, United States of America
Start-End date: 05/10/1998 - 16/10/1998 **Duration:** 10 days
Goals of the stay: Consultant employed by ARM
Provable tasks: Consultant: Optimisation of HDD firmware including servo control algorithm. Training for Cirrus Logic and customers.

Obtained grants and scholarships

1 **Name of the grant:** Ramon y Cajal
Aims: Post-doctoral
Awarding entity: Ministerio de Ciencia e Innovación **Type of entity:** State agency
Conferral date: 01/01/2020 **Duration:** 5 years
End date: 31/12/2024
Entity where activity was carried out: Barcelona Supercomputing Center

2 **Name of the grant:** King's Scholarship
Aims: Pre-doctoral
Awarding entity: King's College, Cambridge
Type of entity: University Centres and Structures and Associated Bodies
Conferral date: 1995
Duration: 1 year
Entity where activity was carried out: University of Cambridge

3 **Name of the grant:** King's Scholarship
Aims: Pre-doctoral
Awarding entity: King's College Cambridge
Type of entity: University Centres and Structures and Associated Bodies
Conferral date: 1994

Other types of collaboration with researchers or technologists

Name principal investigator (PI, Co-PI....): Per Stenstrom
Description of the collaboration: Proofreader for HiPEACinfo Newsletter
Start date: 28/05/2012
Duration: 3 years - 6 months
Relevant results: Proofreader for HiPEACinfo newsletter physically distributed to 500 researchers from academia and industry, and company managers in Europe, America and Asia

Scientific societies and professional associations

1 **Name of the society:** American Association for the Advancement of Science (AAAS)
Start date: 16/09/2017

2 **Name of the society:** Institute of Electrical and Electronics Engineers (IEEE)
Professional category: Member
Start date: 01/01/2004

3 **Name of the society:** Association of Computing Machinery
Professional category: Lifetime Professional Member
Start date: 01/12/2002

Co-operation networks

1 **Name of the network:** 1018.eu
Identification of the network: EuroEXA exploitation
Tasks carried out: Membership secretary
Start date: 31/08/2018

2 **Name of the network:** Full Member
Identification of the network: European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC)
Start date: 30/04/2012

3 **Name of the network:** Member
Identification of the network: Association of Independent Computer Specialists
Start date: 19/05/2003 **Duration:** 2 years

Prizes, mentions and distinctions

1 **Description:** HiPEAC Paper Award 2017
Awarding entity: European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC)
Conferral date: 2017
Recognition linked: Prize recognizing paper in HPCA 2017 (CORE A*). The HiPEAC Paper Award aims to encourage HiPEAC members to publish their work at highly competitive conferences in which Europe is not strongly represented.

2 **Description:** Best paper award
Awarding entity: MEMSYS conference
Conferral date: 06/10/2016
Recognition linked: Best paper award for "Large-Memory Nodes for Energy Efficient High-Performance Computing"

3 **Description:** IEEE Transactions on Computers Featured Article of the Month January 2016
Awarding entity: IEEE Computer Society **Type of entity:** Associations and Groups
Conferral date: 01/2015
Recognition linked: Radojkovic et al is featured paper of the month (of 28 papers published) for January 2016 issue of IEEE Transactions on Computers (CiteScore 2.87, ranked #10/118 in Theoretical Computer Science by Scopus). The article is promoted on the journal's website and is freely available for one month. It is also promoted by videos in English and Chinese.

4 **Description:** Diploma in recognition for Best Student Paper
Awarding entity: UPC Consell Social **Type of entity:** University Centres and Structures and Associated Bodies
City awarding entity: Barcelona, Catalonia, Spain
Conferral date: 01/09/2014

5 **Description:** Best Paper Award
Awarding entity: Third International Workshop on On-chip Memory Hierarchies and Interconnects: Organisation, Management and Implementation
City awarding entity: Porto, Portugal
Conferral date: 25/08/2014

6 **Description:** Best Student Paper Award
Awarding entity: International Conference for High Performance Computing, Networking, Storage and Analysis (SC13) (CORE A)
City awarding entity: Denver, United States of America
Conferral date: 22/11/2013

7 **Description:** Finalist Fundación Repsol Entrepreneurship Fund 2013
Awarding entity: Fundación Repsol
City awarding entity: Madrid, Spain
Conferral date: 22/05/2013

Recognition linked: I was one of the four co-founders of Talaia Systems, an attempted start-up to commercialise the technology from the Mont-Blanc project. We aimed to build high-performance computing systems using mobile system-on-chips, and we had discussions with several vendors and potential investors. Talaia Systems was one of 16 finalists out of 479 projects submitted to Fundación Repsol Entrepreneurship Fund 2013.

8 **Description:** Winner International Science & Engineering Visualisation Challenge (video)
Awarding entity: National Science Foundation and Science Magazine
Conferral date: 01/11/2012
Recognition linked: Narrator of video "Alya Red, a Computational Heart", which received first place.

9 **Description:** HiPEAC Paper Award 2012
Awarding entity: European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC)
Conferral date: 2012
Recognition linked: Prize recognizing paper in MICRO-45 in 2012 (CORE A). The HiPEAC Paper Award aims to encourage HiPEAC members to publish their work at highly competitive conferences in which Europe is not strongly represented.

10 **Description:** HiPEAC Technology Transfer Award
Awarding entity: European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC)
Conferral date: 2012
Recognition linked: Member of the team that received the HiPEAC Technology Transfer Award for the CARMA (CUDA on ARM) development kit

11 **Description:** Best Paper Award
Awarding entity: International Workshop on Systems, Architectures, Modeling, and Simulation (SAMOS Workshop 2009)
City awarding entity: Samos, Greece
Conferral date: 23/07/2009

12 **Description:** King's Scholarship (1995--1996)
Awarding entity: King's College, University of Cambridge
City awarding entity: Cambridge, United Kingdom
Conferral date: 1995
Recognition linked: The King's Scholar (K.S.) is awarded for obtaining a first class in the annual Tripos examination

13 **Description:** King's Scholarship (1994--1995)
Awarding entity: King's College, University of Cambridge **Type of entity:** University
City awarding entity: Cambridge, United Kingdom
Conferral date: 1994
Recognition linked: The King's Scholar (K.S.) is awarded for obtaining a first class in the annual Tripos examination